



**XR-DIMM™**  
**Rugged Memory**  
**SPECIFICATION**  
**(Formerly RS-DIMM)**

**Revision 2.0**

**June 7, 2011**

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## Revision History

Revision	Issue Date	Comments
1.0	2/16/11	Initial Revision
2.0	6/7/11	Changed name to XR-DIMM

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## 1.0 Introduction

### 1.1 Overview

The XR-DIMM (“eXtreme Rugged Dual Inline Memory Module”) Rugged Memory Specification defines a small form factor (38 mm Depth x 67.5 mm Width x 7.36 mm Height) mezzanine DDR3 expansion memory module for use in embedded applications requiring exceptional resistance to shock and vibration as well as extended temperature operation.

The XR-DIMM Rugged Memory Specification includes the board outline, location of mounting holes for positive attachment to the underlying CPU board, connector definition and placement, and pin definition. The XR-DIMM pin definition closely follows the DDR3 SO-DIMM pin definition to ease the implementation of CPU designs which may wish to utilize both expansion memory approaches for differing types of applications.

This specification, like the SO-DIMM specification, supports both unbuffered and registered versions. In addition, the pin definition includes a SATA interface to enable the development of dual function modules containing both DDR3 memory and flash memory for a Solid State Disk (SSD) implementation.

### 1.2 Background

For years, designers of off-the-shelf embedded CPU boards (both SBCs and COMs) for use in rugged applications with significant resistance to shock and vibration have been faced with difficult design decisions for their main memory. Standard memory expansion interfaces such as DIMM and SO-DIMM memory are not designed for these rugged applications. Therefore, significant concern exists about the use of such standard memory expansion approaches.

Designers have responded with two different solutions, each of which has substantial drawbacks. In some cases, an add-on retention mechanism is added to a standard memory expansion installation. Clips, straps, glue or other tie down mechanisms are used to prevent an SO-DIMM from flying out of the socket. However, this approach does not deal with issues relating to the socket itself. Concern continues to exist about movement of the expansion memory module within the socket, causing potential intermittent pin connections and bringing a system down.

Another approach has been to solder memory chips directly to the CPU board. While this approach deals completely with shock and vibration issues, it has three significant drawbacks. The first is the board space consumed by the memory components. As CPU boards shrink in size, this space is extremely valuable. The second is the wide variety in memory requirements for these types

of applications. Each memory configuration must be manufactured individually. The manufacturer is either faced with a large number of SKUs for the different memory configurations (and associated forecasting and inventory issues) or restricting the number of products and perhaps not having a memory configuration appropriate for a particular application requirement. Finally, these CPUs can not upgrade their memory capacity after they are manufactured.

The XR-DIMM approach provides for off-the-shelf, commercially available rugged memory expansion modules of varying capacities, allowing the CPU manufacturer to offer multiple memory size solutions to the OEM customer while maintaining a single CPU SKU. Space on the CPU board is limited to the connector and mounting hole locations. And upgrading memory capacity is as simple as swapping memory modules. Enhanced ruggedness is obtained through the use of a high-performance 240-pin socket connector system and the use of standoffs with screw attachment firmly holding the CPU and memory module together.

### 1.3 Terms and Definitions

- DDP** ..... Dual Die Package
- DDR3** ..... Double Data Rate DRAM 3<sup>rd</sup> generation
- ECC** ..... Error-correcting Code
- XR-DIMM** ..... Rugged Small-outline Dual In-line Memory Module (refers to the common elements of both the unbuffered and registered versions)
- SO-DIMM** ..... Small-outline Dual In-line Memory Module

### 1.4 Feature Summary

- Tiny 67.5 mm x 38 mm x 7.36 mm form factor enables use on a wide variety of small form factor CPU boards
- Full DDR3 implementation with ECC support
- Supports 9-chip or 18-chip implementations up to 4GB
- Supports one or two memory modules per CPU
- Consistent with SO-DIMM pin definitions, easing conversion from SO-DIMM implementations
- Supports registered and unbuffered versions
- Optional SATA interface enables combined RAM and SSD on a single module, reducing system space requirements

- Highly rugged interface to CPU using pin connector and screw attachment, providing enhanced resistance to shock and vibration
- ANSI/VITA 47-2005 shock and vibration compliant

## 1.5 Connector

Samtec BSH/BTH 240-pin connector pair (BSH on the memory module, BTH mate on CPU board).

- Module Side: BSH-120-01-X-D-A
- CPU Board Side: BTH-120-01-X-D-A [change the -01 designation for different stack heights]

## 1.6 Audience

The XR-DIMM Rugged Memory Specification provides information both to the designers of XR-DIMM memory modules and to the designers of CPU boards wishing to incorporate XR-DIMM memory modules.

## 1.7 Related Documentation and Organizations

### **Intel Corporation**

2200 Mission College Blvd.  
Santa Clara, CA 95054-1549

Phone: +1-408-765-8080

<http://www.intel.com>

### **JEDEC**

3103 N. 10th St., Suite 240-S  
Arlington, VA 22201-2107 USA

<http://www.jedec.org>

**SATA**

SATA-IO Administration  
3855 SW 153rd Dr.  
Beaverton, OR 97006 USA

Phone: +1 503-619-0572

Fax: +1 503-644-6708

<http://sata-io.org>

**Samtec, Inc. (Connector data)**

520 Park East Blvd.  
New Albany, IN 47151-1147 USA

Phone: +1-812-944-6733

Fax: +1-812-948-5047

Email: [standards@samtec.com](mailto:standards@samtec.com)

<http://www.samtec.com>

**SFF-SIG**

2784 Homestead Rd. #269  
Santa Clara, CA 95051

Phone: +1-650-961-2473

Email: [info@sff-sig.org](mailto:info@sff-sig.org)

<http://www.sff-sig.org>

## 2.0 Module Connector Interface

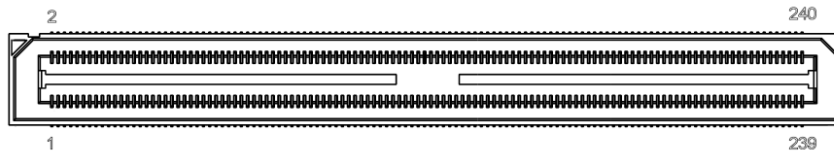
### 2.1 Signal Naming Conventions

Signals follow these naming conventions:

*PREF\_SIG#\_p*

PREF_	Prefix	Empty	Signals for DRAM bus and supply voltages, naming convention follow JEDEC standard for DDR3 Unbuffered DIMM
		SATA_	Signals for SATA option
SIG	Signal		Abbreviation for signal function
#	Number	0,1,...n	Index of a multibit bus or multiple signal copy
_p	Polarity	Empty	Signal without active polarity or active high
		_n	Signal with active low polarity
		_t	True signal of a differential signal pair
		_c	Complement signal of a differential signal pair

#### Socket Outline BSH-120-01-X-D-A (view on connector)



## 2.2 Signal Functional Description

### XR-DIMM Signal Description

Symbol	Type	Polarity	Function
A0–A15	IN	—	During a Bank Activate command cycle, address input defines the row address (RA0–RA15). During a Read or Write command cycle, address input defines the column address. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0, BA1, BA2 defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0, BA1, BA2 to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0, BA1 or BA2. If AP is low, BA0, BA1 and BA2 are used to define which bank to precharge. A12(BC_n) is sampled during READ and WRITE commands to determine if burst chop (on-the-fly) will be performed (HIGH, no burst chop; LOW, burst chopped).
BA0–BA2	IN	—	Selects which SDRAM bank of eight is activated.
CK0_t–CK1_t CK0_c–CK1_c	IN	Differential crossing	CK_t and CK_c are differential clock inputs. All the DDR3 SDRAM addr/ctrl inputs are sampled on the crossing of positive edge of CK_t and negative edge of CK_c. Output (read) data is referenced to the crossing of CK_t and CK_c (Both directions of crossing).
CKE0–CKE1	IN	Active High	Activates the SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode, or the Self Refresh mode.
DM0–DM8	IN	Active High	DM is an input mask signal for write data. Input data is masked when DM is sampled High coincident with that input data during a write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading.
DQ0–DQ63, CB0–CB7	I/O	—	Data and Check Bit Input/Output pins.
DQS0_t–DQS8_t DQS0_c–DQS8_c	I/O	Differential crossing	Data strobe for input and output data. For raw cards using x16 organized DRAMs, Pins DQ0–DQ7 are associated with the LDQS_t and LDQS_c pins and Pins DQ8–DQ15 are associated with UDQS_t and UDQS_c pins.
ODT0–ODT1	IN	Active High	When high, termination resistance is enabled for all DQ, DQS_t, DQS_c and DM pins, assuming this function is enabled on the DRAM.
PAR_IN	IN	—	XR-RDIMM only: Parity bit for the Address and Control bus. ("1": Odd, "0": Even)
ERR_OUT_n	OUT (open drain)	Active Low	RS_RDIMM only: Parity error detected on the Address and Control bus. A resistor may be connected from Err_Out_n bus line to VDD on the system planar to act as a pull up.
RAS_n, CAS_n, WE_n	IN	Active Low	RAS_n, CAS_n, and WE_n (along with S_n) define the command being entered.
RESET_n	IN	Active Low	The RESET_n pin is connected to the RESET_n pin on each DRAM. When low, all DRAMs are set to a known state. For XR-RDIMM the reset signal also puts the register into a defines state
S0_n–S3_n	IN	Active Low	Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. This signal provides for external rank selection on systems with multiple ranks.
VDD, VSS	Supply		Power and ground for the DDR3 SDRAM input buffers, and core logic. VDD and VDDQ pins are tied to VDD/VDDQ planes on these modules.
VDDQ	Supply		Power supply for the DDR3 SDRAM output buffers to provide improved noise immunity. For the unbuffered DDR3 XR-DIMM designs, VDDQ shares the same power plane as VDD pins.
VTT	Supply		Termination voltage for C/A & Control bus, by default at VDD/2
VDDSPD	Supply		Power supply for SPD EEPROM. This supply is separate from the VDD/VDDQ power plane. EEPROM supply is operable from 3.0V to 3.6V.
VREFDQ	Supply		Reference voltage for I/O inputs, by default at VDD/2
VREFCA	Supply		Reference voltage for command/address/control inputs, by default at VDD/2
SA0–SA2	IN	—	These signals are tied at the system planar to either VSS or VDDSPD to configure the serial SPD EEPROM address range.

SDA	I/O	—	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. An external resistor may be connected from the SDA bus line to VDDSPD to act as a pullup on the system board.
SCL	IN	—	This signal is used to clock data into and out of the SPD EEPROM. An external resistor may be connected from the SCL bus time to VDDSPD to act as a pullup on the system board.
EVENT_n	Output (Open Drain)	Active Low	This signal indicates that a thermal event has been detected in the thermal sensing device. The system should guarantee the electrical level requirement is met for the EVENT_n pin on the TS/SPD part.
NC(TEST)			Used by memory bus analysis tools (unused (NC) on memory module)
NC			Not connected
SATA_RX_p SATA_RX-n	OUT	Differential	Differential SATA Receive signal pair
SATA_TX_p SATA_TX-n	IN	Differential	Differential SATA Transmit signal pair

## 2.3 Pin Assignment

### XR-DIMM Pin Configuration - Odd Row

Odd Row									
Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
1	VSS	49	DQS2_t	97	CKE0	145	S1_n	193	DQ49
3	VSS	51	VSS	99	VDD	147	ODT1	195	VSS
5	DQ0	53	DQ18	101	BA2	149	VDD	197	DQS6_c
7	DQ1	55	DQ19	103	VDD	151	S3_n/NC	199	DQS6_t
9	VSS	57	VSS	105	A11	153	VSS	201	VSS
11	DQS0_c	59	DQ24	107	A7	155	DQ32	203	DQ50
13	DQS0_t	61	DQ25	109	VDD	157	DQ33	205	DQ51
15	VSS	63	VSS	111	A5	159	VSS	207	VSS
17	DQ2	65	DQS3_c	113	A4	161	DQS4_c	209	DQ56
19	DQ3	67	DQS3_t	115	VDD	163	DQS4_t	211	DQ57
21	VSS	69	VSS	117	A2	165	VSS	213	VSS
23	DQ8	71	DQ26	119	VDD	167	DQ34	215	DQS7_c
25	DQ9	73	DQ27	121	CK1_t	169	DQ35	217	DQS7_t
27	VSS	75	VSS	123	CK1_n	171	VSS	219	VSS
29	DQS1_c	77	CB0	125	VDD	173	DQ40	221	DQ58
31	DQS1_t	79	CB1	127	VREFCA	175	DQ41	223	DQ59
33	VSS	81	VSS	129	PAR_IN	177	VSS	225	VSS
35	DQ10	83	DQS8_c	131	VDD	179	DQS5_c	227	SA2
37	DQ11	85	DQS8_t	133	A10/AP	181	DQS5_t	229	VSS
39	VSS	87	VSS	135	BA0	183	VSS	231	SATA_RX_p
41	DQ16	89	CB2	137	VDD	185	DQ42	233	SATA_RX_n
43	DQ17	91	CB3	139	WE_n	187	DQ43	235	VSS
45	VSS	93	VSS	141	CAS_n	189	VSS	237	VTT
47	DQS2_c	95	VTT	143	VDD	191	DQ48	239	VTT

## XR-DIMM Pin Configuration - Even Row

Even Row									
Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol	Pin#	Symbol
2	VSS	50	DM2	98	CKE1	146	VDD	194	VSS
4	VSS	52	VSS	100	VDD	148	ODT0	196	DM6
6	DQ4	54	DQ22	102	A15	150	A13	198	VSS
8	DQ5	56	DQ23	104	A14	152	VDD	200	DQ54
10	VSS	58	VSS	106	VDD	154	S2_n/NC	202	DQ55
12	DM0	60	DQ28	108	A12/BC	156	VSS	204	VSS
14	VSS	62	DQ29	110	A9	158	DQ36	206	DQ60
16	DQ6	64	VSS	112	VDD	160	DQ37	208	DQ61
18	DQ7	66	DM3	114	A8	162	VSS	210	VSS
20	VSS	68	VSS	116	A6	164	DM4	212	DM7
22	DQ12	70	DQ30	118	VDD	166	VSS	214	VSS
24	DQ13	72	DQ31	120	A3	168	DQ38	216	DQ62
26	VSS	74	VSS	122	A1	170	DQ39	218	DQ63
28	DM1	76	CB4	124	VDD	172	VSS	220	VSS
30	VSS	78	CB5	126	CKO_t	174	DQ44	222	VDDSPD
32	DQ14	80	VSS	128	CKO_c	176	DQ45	224	SA0
34	DQ15	82	DM8	130	VDD	178	VSS	226	SA1
36	VSS	84	VSS	132	EVENT_n	180	DM5	228	SCL
38	DQ20	86	CB6	134	A0	182	VSS	230	SDA
40	DQ21	88	CB7	136	VDD	184	DQ46	232	VSS
42	VSS	90	VSS	138	BA1	186	DQ47	234	SATA_TX_n
44	VREFDQ	92	RESET_n	140	VDD	188	VSS	236	SATA_TX_p
46	NC (TEST)	94	ERR_OUT_n	142	RAS_n	190	DQ52	238	VSS
48	VSS	96	VTT	144	S0_n	192	DQ53	240	VTT

### 3.0 Electrical Specification

#### 3.1 Six Layer Board (9-chip module)

##### 3.1.1 Stack-up

Layer	Board stackup	Thickness	Cu weight
Mask		0.015 mm	
L1 Copper	Signal	0.045 mm	0.5 oz + Plating
Prepreg		0.10 mm	
L2 Copper	Vdd/Vss	0.03 mm	1.0 oz
Prepreg		0.127 mm	
L3 Copper	Signal	0.03 mm	1.0 oz
Prepreg		0.34 mm	
L4 Copper	Signal	0.03 mm	1.0 oz
Prepreg		0.127 mm	
L5 Copper	Vdd/Vss	0.03 mm	1.0 oz
Prepreg		0.10 mm	
L6 Copper	Signal	0.045 mm	0.5 oz + Plating
Mask		0.015 mm	

Overall Thickness (without Mask) = 1.0 mm +/-0.1mm

##### 3.1.2 Impedance

**6-Layer Geometry/Impedance Table**

Layer	Single Ended		Differential	
	Width	Target Z0	Width/Space	Target Zdiff
L1 / L6	0.1 mm	60 ohms ±10%	0.1 / 0.1 mm	88 ohms ±15%
	0.2 mm	45 ohms ±10%	0.2 / 0.1 mm	68 ohms ±15%
L3	0.1 mm	60 ohms ±10%	0.1 / 0.1 mm	88 ohms ±15%
	0.2 mm	45 ohms ±10%	0.2 / 0.1 mm	68 ohms ±15%
L4	0.1 mm	60 ohms ±10%	0.1 / 0.1 mm	88 ohms ±15%
	0.2 mm	45 ohms ±10%	0.2 / 0.1 mm	68 ohms ±15%

1. All trace widths are subject to adjustment by PCB vendor, as required to align impedance targets.
2. Only the 60 ohm single ended impedances are firm specifications.
3. All other impedance targets are provided for reference only.

### 3.1.3 Power and Ground Planes

Most DIMM printed circuit board designs use six layers of glass epoxy material. PCBs should contain solid ground plane layers as far as possible. The PCB stack-up must be designed with 0.10 mm wide traces. Layer 2 and 5 are divided for the plane referencing (the signals on the signal layer and its referencing plane on GND/ $V_{DD}$  layer are adjacent to each other).

### 3.1.4 AC/DC Signal Specifications

<b>DC Signal Specification</b>		
Attribute	Values (typical)	Notes
Voltage options	1.5 Volt $V_{DD}/V_{DDQ}$	All DDR3 modules use a common $V_{DD}/V_{DDQ}$ power plane. $V_{DD}$ and $V_{DDQ}$ are tied together on the XR-DIMM
Serial PD voltage options	3.0 Volt to 3.6 Volt $V_{DDSPD}$	$V_{DDSPD}$ is not tied to $V_{DD}$ or $V_{DDQ}$ on the XR-DIMM
Interface	1.5 Volt signalling	
Reference voltage for I/O inputs $V_{DDQ}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
Reference voltage for command/address/control inputs $V_{DDCA}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
Termination reference voltage $V_{TT}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
<b>AC Signal Specification</b>		
Input /Output AC logic level, capacitance, and timing parameters vary based on DRAM components used. Refer to module manufacturer specification for complete AC value details.		

## 3.2 Eight Layer Board (18-chip module)

### 3.2.1 Stack-up

Layer	Board stackup	Thickness	Cu weight
Mask		0.015 mm	
L1 Copper	Signal	0.03 mm	0.5 oz + Plating
Prepreg		0.09 mm	
L2 Copper	Vdd/Vss	0.017 mm	0.5 oz
Prepreg		0.115 mm	
L3 Copper	Signal	0.017 mm	0.5 oz
Prepreg		0.20 mm	
L4 Copper	Vdd/Vss	0.017 mm	0.5 oz
Prepreg		0.10 mm	
L5 Copper	Signal	0.017 mm	0.5 oz
Prepreg		0.20 mm	
L6 Copper	Signal	0.017 mm	0.5 oz
Prepreg		0.10 mm	
L7 Copper	Vdd/Vss	0.017 mm	0.5 oz
Prepreg		0.09 mm	
L8 Copper	Signal	0.03 mm	0.5 oz + Plating
Mask		0.015 mm	

Overall Thickness (without Mask) = 1.0 mm +/-0.1mm

NOTE:  
Even if you need to adjust the stackup, the distance between L5 and L6 should be kept >0.2 mm to reduce the crosstalk between L5 and L6 traces.

### 3.2.2 Impedance

**8- Layer Geometry/Impedance Table**

Layer	Single Ended		Differential	
	Width	Target Z0	Width/Space	Target Zdiff
L1 & L8	0.09 mm	60 ohms ±10%	0.09 / 0.1 mm	95 ohms ±15%
	0.15 mm	44 ohms ±10%	0.15 / 0.1 mm	72 ohms ±15%
L3, L5 & L6	0.075 mm	60 ohms ±10%	0.075 / 0.1 mm	100 ohms ±15%
	0.15 mm	44 ohms ±10%	0.15 / 0.1 mm	75 ohms ±15%

1. All trace widths are subject to adjustment by PCB vendor, as required to align impedance targets.  
2. Only the 60 ohm single ended impedances are firm specifications.  
3. All other impedance targets are provided for reference only.

### 3.2.3 Power and Ground Planes

PCBs should contain solid ground plane layers as far as possible. The PCB stack-up must be designed with 0.10 mm wide traces. Layer 2 and 5 are divided for the plane referencing (the signals on the signal layer and its referencing plane on GND/ $V_{DD}$  layer are adjacent to each other). Layer 4 is a solid  $V_{DD}$  plane. Any exceptions to these design rules will be identified in the appendix for that raw card.

### 3.2.4 AC/DC Signal Specifications

<b>DC Signal Specification</b>		
Attribute	Values (typical)	Notes
Voltage options	1.5 Volt $V_{DD}/V_{DDQ}$	All DDR3 modules use a common $V_{DD}/V_{DDQ}$ power plane. $V_{DD}$ and $V_{DDQ}$ are tied together on the XR-DIMM
Serial PD voltage options	3.0 Volt to 3.6 Volt $V_{DDSPD}$	$V_{DDSPD}$ is not tied to $V_{DD}$ or $V_{DDQ}$ on the XR-DIMM
Interface	1.5 Volt signalling	
Reference voltage for I/O inputs $V_{DDQ}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
Reference voltage for command/address/control inputs $V_{DDCA}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
Termination reference voltage $V_{TT}$	$0.5 \times V_{DD}$	This is typical value. Refer to module manufacturer specification for minimum, maximum, and actual values
<b>AC Signal Specification</b>		
Input /Output AC logic level, capacitance, and timing parameters vary based on DRAM components used. Refer to module manufacturer specification for complete AC value details.		

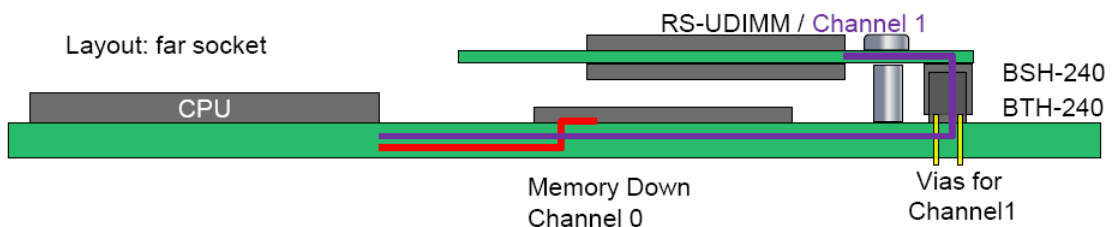
## 4.0 CPU Board Layout Guidelines

This section is derived from Intel's design and motherboard layout recommendations contained in the following two documents:

- Capella Design Guide Revision 2.1 (Document #398905)
- Arrandale EDS Vol. 1 of 2, Revision 2.1 (Document #416056)

These guidelines are specific to an unbuffered XR-DIMM implementation.

Layout guidelines are based on a module orientation with respect to the CPU / chipset placement as shown in *Figure 1* below. The figure also shows potential placement for an additional channel of soldered memory on the CPU board.



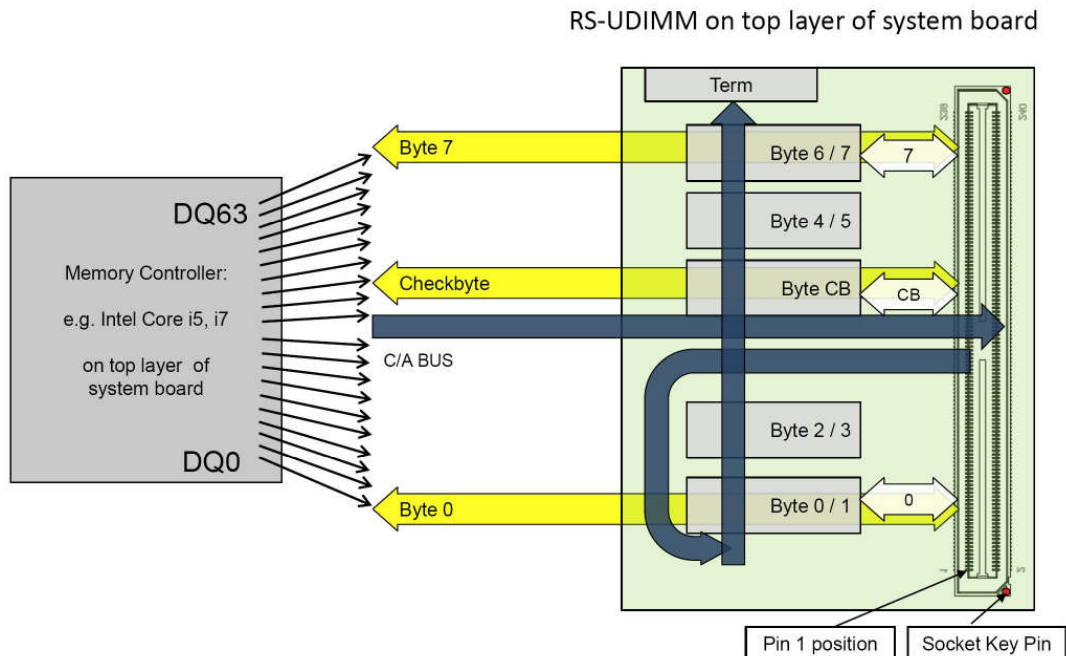
**Figure 1. Module orientation on CPU board vis-à-vis processor / chipset**

### 4.1 DDR3 Signal Groups

The table below provides the signal group description for the DDR3 memory interface. *Figure 2* shows a high level routing overview when the module is oriented as shown in *Figure 1*.

Signal Name	Description
<b>Dual-channel – Data Signal Group</b>	
DM0–DM8	Data Mask
DQ0–DQ63, CB0–CB7	Data Bus
DQS0_t–DQS8_t, DQS0_c–DQS8_c	Data Strobe
<b>Dual-channel – Command Signal Group</b>	
A0–A15	Memory Address Bus
BA0–BA2	Bank Select
RAS_n, CAS_n, WE_n	Address Selects and Write Enable
<b>Dual-channel – Control Signal Group</b>	
S0_n–S3_n	Chip Select
CKE0–CKE1	Clock Enable
ODT0–ODT1	On-die Termination

Dual-channel – Clock Signal Group	
CK0_t–CK1_t, CK0_c–CK1_c	Memory Clock



**Figure 2. Routing overview with module placement in *Figure 1***

## 4.2 Length Constraints

There are two levels of length constraints placed on each signal group within the interface:

- Absolute length constraints
  - The absolute length constraints are provided in the constraint tables for each signal group. These constraints define the length range over which signals meet signal integrity rules. A subset of this solution space is then defined via a set of clock length matching formulas, defined to ensure the clock relative AC timing margins. These two sets of overlapping length constraints then determine the final routing solution space for a particular platform design.
  - Perform a preliminary test route to establish the natural bounds on all signal groups. Once established, the target lengths for each XR-DIMM clock group can then be defined such that an acceptable solution space is available when length matching formulas are applied.
- Clock length matching requirements

- The clock target length is typically constrained on the low end by the control to clock length matching rules, and constrained on the high end by the strobe to clock rules and the need to minimize data and strobe serpentine. The recommended approach consists of two steps:
  1. Determine the length of the longest control signal for each XR-DIMM in the test route and then define the clock target length for each XR-DIMM as short as possible while still ensuring the control trace lengths meet the control to clock length matching rule.
  2. Allow the command bus to be routed easily within the more relaxed command to clock length matching rules, which minimizes DQ/DQS serpentine requirements. The clock target length should also be checked to make sure the longest DQ/DQS byte lanes fall within the resulting length formulas. Additionally, DQ to DQS length matching constraints should also be met.
- For optimal timing margins, all clocks to a particular XR-DIMM connector should be length tuned to the target length for that XR-DIMM.

### 4.3 Layer Utilization

- Individual signal groups may be partitioned between routing layers in any manner necessary to facilitate motherboard routing.
- Individual byte lanes must be routed as a group on the same layer so as to minimize data to strobe skew.
- Ensure reference plane transition vias are located in close proximity (within 150 mils/3.81 mm) of signal transition vias whenever signals are routed on multiple layers, such that the associated return currents can transition between reference planes.
- Command signal groups can be routed on outer microstrip layers if required to complete the route, though it may not be optimal. In all cases, the individual signal groups should be routed as a group on either inner or outer layers.
- Each data channel can be treated as eight separate and independent byte lanes for routing. Byte lanes may be partitioned between internal routing layers as required to complete the route. It is required that each byte lane signal set be routed as a group on the same layer to minimize skew within the byte lane.
- Reference planes must be continuous so that return currents can image the signal trace over the entire path. Routing over power plane partitions or voids is not allowed.
- GND reference for Data Group is recommended while Command Group, Control Group and CLK Group reference to  $V_{CC}$ .

- It is required that a minimum of four AC decoupling caps be located at the  $V_{DD}$  pins of each SO-DIMM connector in the vicinity of the CMD, Clock and Control signals. The decoupling caps are used to provide a path for the return current to migrate to the motherboard GND layer and complete the path back to the processor. These four caps can be shared by the clock, control and command signals. A capacitor value of 0.1 $\mu$ F is recommended. The four capacitors should be placed on the same side of the motherboard as the XR-DIMM connector.

## 4.4 Length Matching and Length Formulas

The routing guidelines define the recommended routing topologies, trace width and spacing geometries, and absolute minimum and maximum routed lengths for each signal group, which are recommended to achieve optimal signal integrity and timing margins. Length matching formulas provide more length matching restrictions for each signal group, further restricting the clock length.

All signal groups are length matched to the DDR3 clocks, with the clocks themselves being length tuned to a fixed length across each XR-DIMM connector. The amount of minimum to maximum length variance allowed for each group around the clock reference length varies from signal group to signal group depending on the amount of timing variance that can be tolerated.

A simplified summary of the length matching formulas for each signal group is provided below. This table also defines the DQ to DQS matching rules, which are imposed across each byte lane.

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock – 0.5" (12.7 cm)	Clock + 0.0"
Command-to-Clock	Clock – 0.5" (12.7 cm)	Clock + 0.5" (12.7 cm)
Strobe-to-Clock	Clock – 0.5" (12.7 cm)	Clock + 1.0" (25.4 cm)
Data-to-Strobe (per byte lane)	Strobe – 20 mils (0.508 mm)	Strobe + 20 mils (0.508 mm)

**Note:** All length matching formulas are based on processor die-pad to XR-DIMM pin total length.

Package length compensation is an integral part of the overall length matching process and is important within individual byte lanes due to the stringent data to strobe length matching requirements within each byte lane.

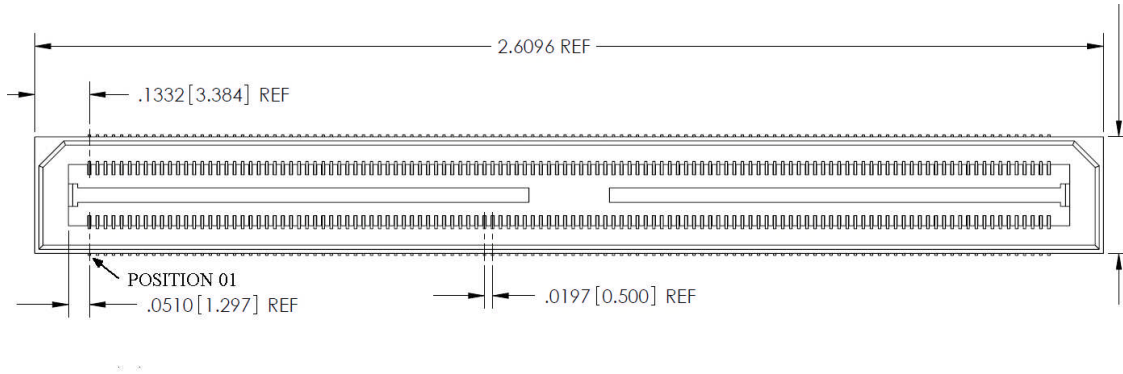
Contact your chip vendor for detailed tables on internal package lengths.

Recommended routing topologies, trace width and spacing geometries and thus resulting impedances are mainly related to the memory controller that is used. Please ask your chip vendor for a detailed design guideline. You may use guidelines for a DDR3 SO-DIMM connector design if no guideline for XR-DIMM is provided.

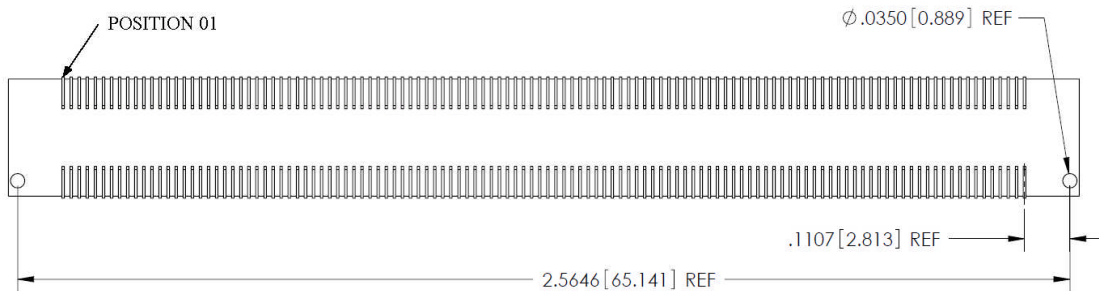
## 5.0 Mechanical Specifications

### 5.1 Connector on Memory Module (BSH-120-01-X-D-A)

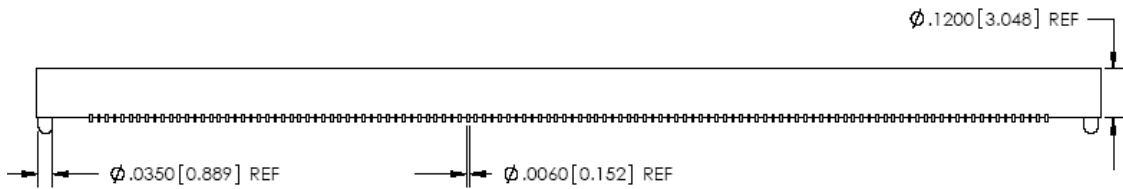
#### Top View



#### Bottom View

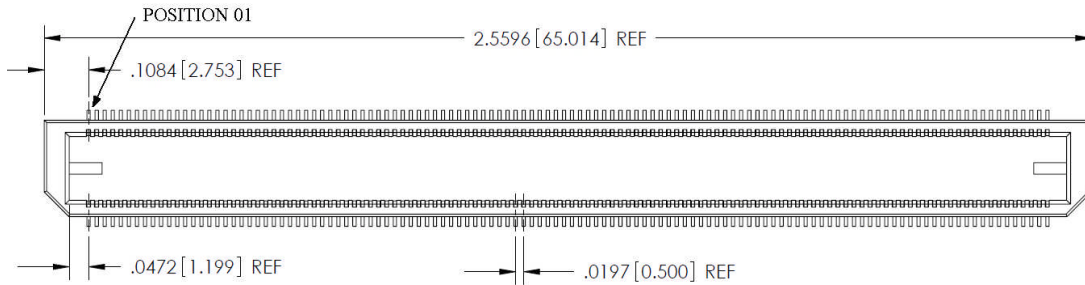


#### Front View

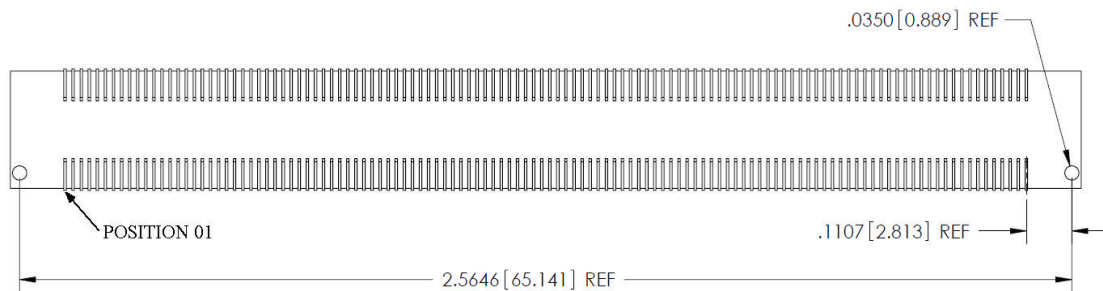


## 5.2 Connector on CPU Board (BTH-120-01-X-D-A)

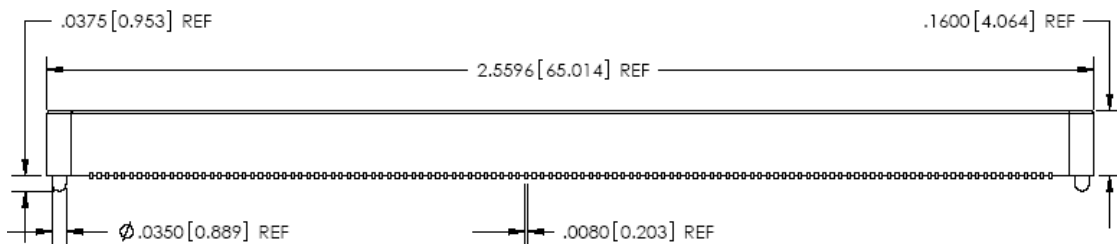
### Top View



### Bottom View

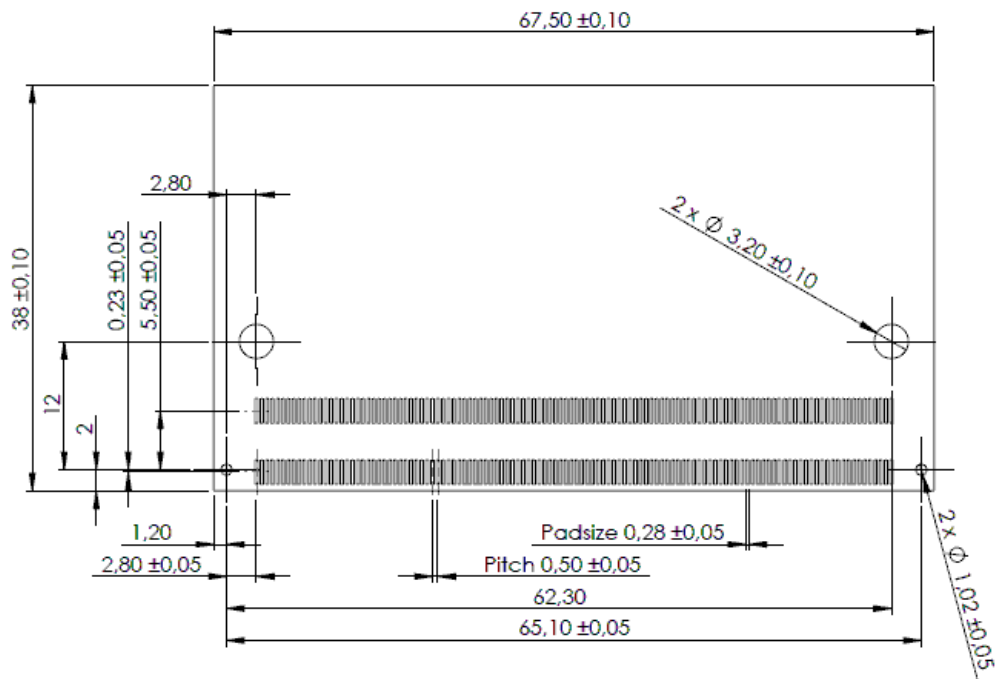


### Front View

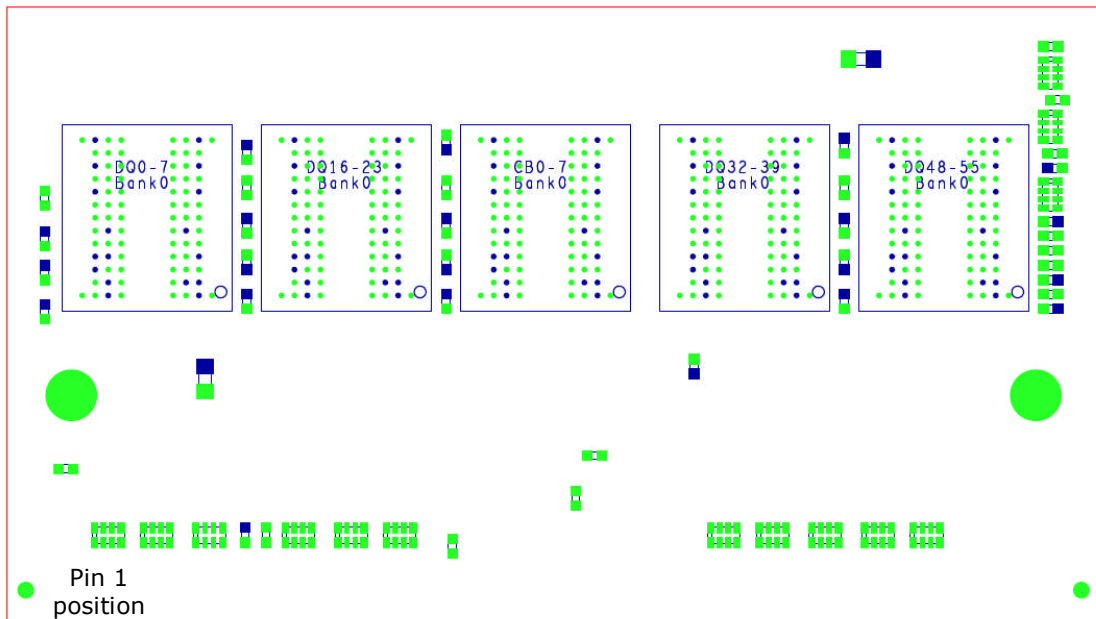


### 5.3 Module Mechanical View

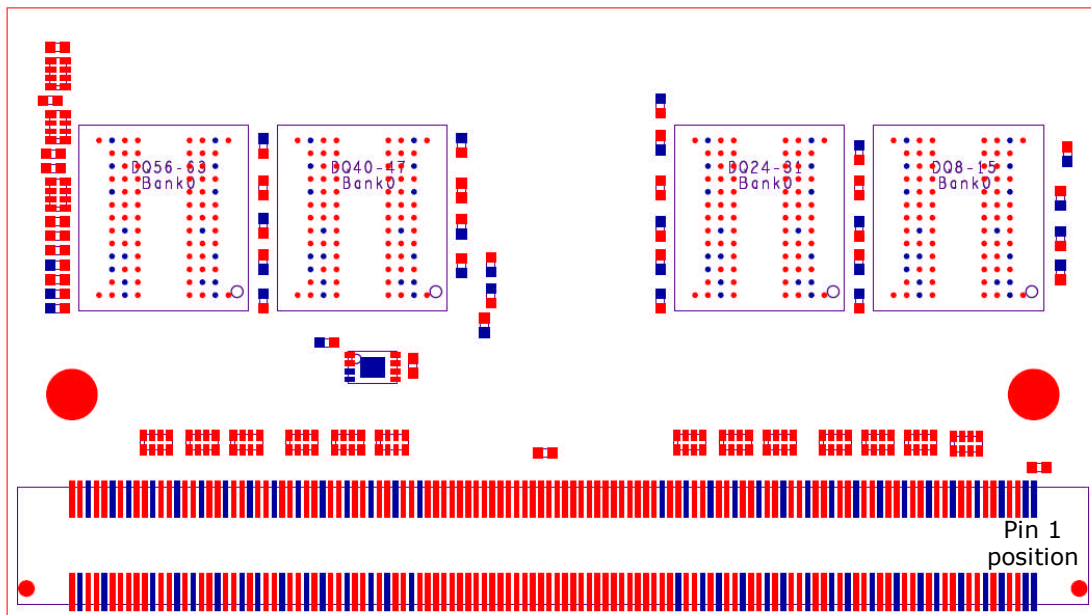
**Module Outline** (all dimensions are in mm)



## Module Layout -Top View



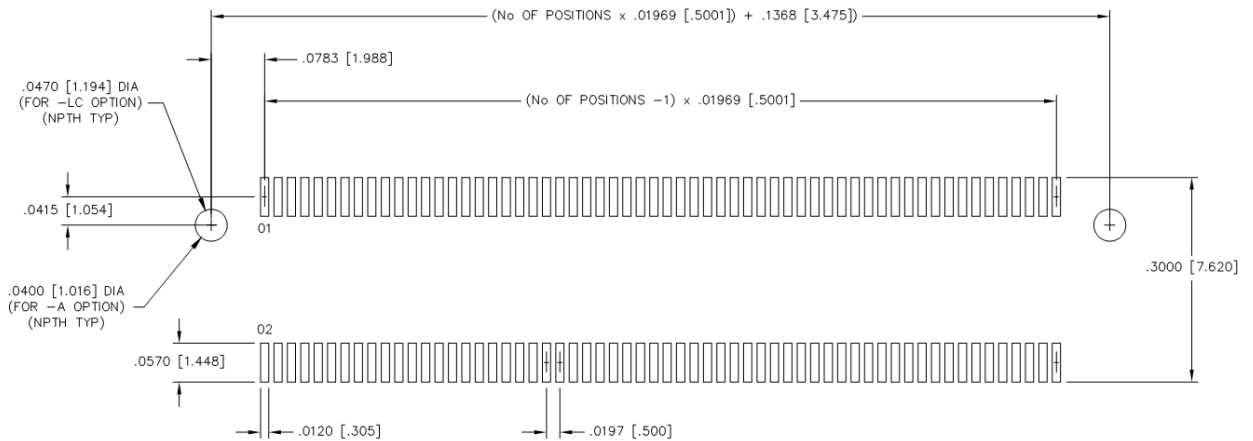
## Module Layout - Bottom View (mirrored)



## 5.4 Connector Footprints

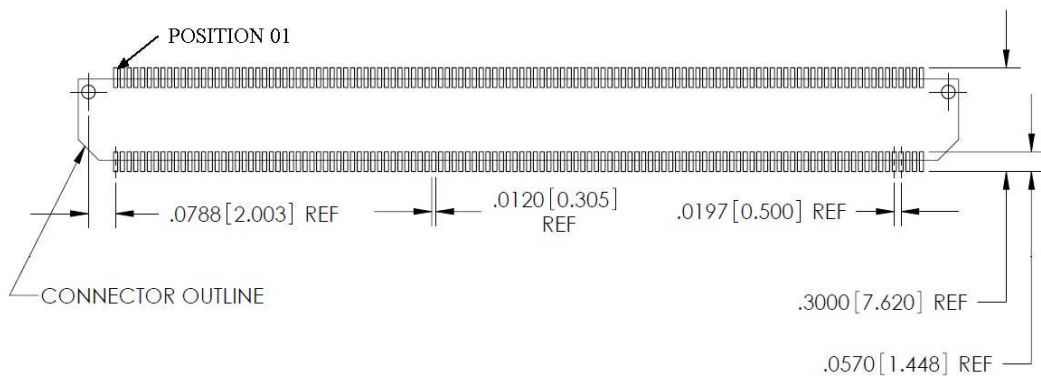
### BSH Connector Footprint - Module Bottom View

This view defines the male terminal connector footprint on the bottom of the memory module. Locate per the *Module Layout - Bottom View* drawing above.



### BTH Connector Footprint - CPU View

This view defines the female terminal connector footprint on the CPU board.

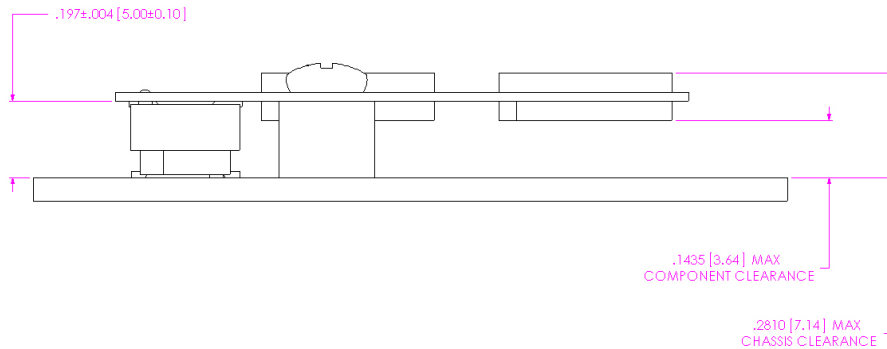


## 5.5 Component Height Under Module

The clearance between the memory module and the CPU board noted below is the worst case situation when DDP (Dual Die Package) DRAM

is used on the module. If a heat spreader is used on the memory module, additional clearance will be needed. Component height under the module should be restricted to provide clearance and sufficient room for airflow.

Inches [mm]  
Tolerance:  $\pm 0.004$  [0.10]



## 5.6 Standoffs

Many variations of standoffs are permissible. These recommendations are here not to overly constrain the possible design solutions; but to insure the reliability of the XR-DIMM. Of primary importance are the 5 mm height and the M2 thread.

**Hex-Standoff / Female - Female / Thread I-1/Inside: M2** [or English equivalent]  
Brass QQ-B-6261 ASTM-B-16 / Nickel plated / Length: 5.0 mm Hex Sizes or Dia.: 4 SW Tolerance:  $-0.000'' + 0.006''$  [-0.00 mm/+0.1524 mm]

**Machine Screw Pan Head Phillips DIN 7985 - ISO 7045** Length 4.0 mm  
Material Stainless Steel ASTM-A-581 Thread M2 Head Dia. 4.0 mm Type Machine Screws DIN Head Height 1.60 mm Design Phillips Head Model DIN 7985 / ISO 7085 Pan Head RoHS compliant



## 5.7 Mounting & Processing

These guidelines are recommended or suggested to ensure reliability of the module to CPU connection. Equivalent or better solutions are permissible.

### **Loctite 2701 - Specifications**

Basic Ingredients	Dimethacrylate Ester
Color	Green
Cure Time	6 hrs.
Pack Size	50 ml
Pack Type	Bottle
Primary Application Category	Threadlocking
Product Category	Anaerobic
Secondary Application	Metal Fasteners
Strength	High