SUMIT™

Stackable Unified Module Interconnect Technology™

SPECIFICATION

Revision 1.3

February 18, 2009

IMPORTANT INFORMATION AND DISCLAIMERS

The Small Form Factor Special Interest Group, Inc. (SFF-SIG) does not make any warranties with regard to this Stackable Unified Module Interconnect Technology (SUMIT) specification ("Specification") and in particular, neither warrants nor represents that this specification nor any products made in conformance with it will work in the intended manner. Nor does the SFF-SIG assume responsibility for any errors that the Specification may contain or have any liabilities or obligations for damages including, but not limited to, special, incidental, indirect, punitive, or consequential damages whether arising from or in connection with the use of this specification in any way.

No representation or warranties are made that any product based in whole or part on this Specification will be free from defects or safe for use for its intended purposes. Any person making, using, or selling such product does so at his or her own risk.

THE USER OF THIS SPECIFICATION HEREBY EXPRESSLY ACKNOWLEDGES THAT THE SPECIFICATION IS PROVIDED "AS IS", AND THAT THE SFF-SIG MAKES NO REPRESENTATIONS, EXTENDS ANY WARRANTIES OF ANY KIND, EITHER EXPRESS OR IMPLIED, ORAL, OR WRITTEN, INCLUDING ANY WARRANTY OF MERCHANTABILITY OR FITNESS FOR ANY PARTICULAR PURPOSE, OR WARRANTY OR REPRESENTATION THAT THE SPECIFICATION OR ANY PRODUCT OR TECHNOLOGY UTILIZING THE SPECIFICATION OR ANY SUBSET OF THE SPECIFICATION WILL BE FREE FROM ANY CLAIMS OF INFRINGEMENT OF ANY INTELLECTUAL PROPERTY, INCLUDING PATENTS, COPYRIGHT AND TRADE SECRETS NOR DOES THE SFF-SIG ASSUME ANY RESPONSIBILITIES WHATSOEVER WITH RESPECT TO THE SPECIFICATION OR SUCH PRODUCTS. THE SFF-SIG DISCLAIMS ALL LIABILITY, INCLUDING LIABILITY FOR INFRINGEMENT OF ANY PROPRIETARY RIGHTS RELATING TO USE OF INFORMATION IN THIS SPECIFICATION. NO LICENSE, EXPRESS OR IMPLIED BY ESTOPPEL, OR OTHERWISE, TO ANY INTELLECTUAL PROPERTY RIGHTS IS GRANTED HEREIN.

Designers must not rely upon the absence or characteristics of any features marked "reserved". The SFF-SIG reserves these for future definition and shall have no responsibility whatsoever for conflicts or incompatibilities arising from future changes to them.

All product names and trademarks, registered trademarks, or service marks are property of their respective owners.

Please send comments via electronic mail to *info@sff-sig.org*.

Revision History

Revision	Issue Date	Comments
0.11	N/A	Initial internal working document
0.21	N/A	Initial internal working document
0.22	01.18.08	Initial internal working document
0.23	02.04.08	Updates to Section 4
0.24	02.18.08	Miscellaneous clean up
0.90	02.22.08	Removal of two USB channels and changing USB 0/1 pin locations
0.91	03.03.08	Add back USB Channel 2
1.00	04.05.08	Final approved with clean up
1.1	12.09.08	Added additional USB and USB control, clarified pin context
1.3	02.18.09	Added LPC DMA support, defined four optional x1 PCIe lanes from the PCIe x4 lane and defined 22 mm stack height for SBCs

Table of Contents

1.0 Introduction

1.1 General

SUMIT™ is an electromechanical connectorization specification that integrates common high-speed and low-speed serial and legacy expansion buses for next generation small form factor products. It is a stackable, I/O-centric expansion approach that is form-factor independent. The purpose is to provide a compact, stackable, multi-board I/O expansion solution for future embedded systems designs which are suitable for industrial environments.

SUMIT can be used to support a single mezzanine card or to allow multiple boards on a stack. It is designed to be processor independent since it focuses on bus and interconnect technology rather than any single processor, DSP, or microcontroller architecture.

The SUMIT acronym stands for Stackable Unified Module Interconnect Technology™ and is pronounced "Sum it".

In a single connector, SUMIT supports one x1 (pronounced "by one") PCI Express™ lane, four high-speed USB 2.0 channels, LPC (Low Pin Count) Bus, SPI/uWire, SMBus/I²C Bus, and ExpressCard™ signaling on a single, tiny, high-speed connector. A second identical connector supports one additional x1 PCI Express lane, one x4 ("by four") PCI Express lane plus additional power, ground, and control signals. The second connector is for applications requiring more channels and higher bandwidth. The PCIe x4 lane can alternatively support four PCIe x1 lanes for a total of six PCIe x1 lanes with both SUMIT connectors.

SUMIT A Connector
- One PCIe x1 Lane
- Four USB 2.0
- ExpressCard
- Low Pin Count Bus (LPC)
- SPI.uWire
- SMBus/I²C Bus

SUMIT B Connector
- One PCIe x1 Lane
- One PCIe x4 *or* four PCIe x1 Lanes

The SUMIT connectors also contain +12V, +5V, +5V standby, +3V and grounds. There are also other control and status signals included.

1.2 Audience

This document is written for design engineers that desire to understand the basics of SUMIT. It does not specify the connector mounting location or application of the technology to any specific computer module or I/O board. That

information will be provided and explained in the specification that governs the implementation of SUMIT technology on the particular form-factor.

Since SUMIT supports high-speed serial bus signals, care must be exercised with respect to best layout practice for high-speed signals. Please reference the websites listed in the next section for their design recommendations. Also visit the SFF-SIG website for application notes or design guides that may be available.

1.3 Related Documents and Organizations

ExpressCard Specification
PCMCIA
2635 North First Street
Suite 218
San Jose, CA 95134 USA
Phone: +1-408-433-2273
Fax: +1-408-433-9558
www.expresscard.org

I²C Specification
NXP Semiconductors Netherlands B.V. (formerly Philips Semiconductors)
Eindhoven, Netherlands
http://www.nxp.com/acrobat_download/literature/9398/39340011.pdf

Low Pin Count (LPC) Specification
Intel Corporation
Santa Clara, CA USA
http://www.intel.com/design/chipsets/industry/lpc.htm

PCI Express Specification
PCI-SIG
3855 SW 153rd Drive
Beaverton, OR 97006 USA
Phone: +1-503-619-0569
Fax: +1-503-644-6708
www.pcisig.com

Samtec, Inc. (Connector data)
520 Park East Boulevard
New Albany, IN 47151-1147 USA
Phone: +1-812-944-6733
Fax: +1-812-948-5047
www.samtec.com

SFF-SIG
Small Form Factor Special Interest Group
2784 Homestead Road #269
Santa Clara, CA 95051 USA
Phone: +1-650-961-2473
www.sff-sig.org

SMBus Specification
System Management Interface Forum, Inc.
100 N. Central Expressway
Suite 600
Richardson, Texas 75080-5323 USA
Fax: +1-972-238-1286
www.smbus.org

SPI
The SPI bus is a *de facto* standard, rather than one agreed by any international committee. The reason for this is its essential simplicity. The best reference is http://www.freescale.com/files/microcontrollers/doc/ref_manual/S12SPIV3.pdf

USB
USB Implementers Forum, Inc.
3855 SW 153rd Drive
Beaverton, OR 97006
www.usb.org

2.0 Acronyms and Terms

ATX-style — Refers to the power supply configuration that allows the computer to be turned off via software. ATX power supplies have two separate five volt signals, one that powers up and down with the system (+5V) and one that stays powered all of the time unless the supply is disconnected from the system power(+5VSB, standby) in order for the system to be capable of waking up from network traffic, keyboard, etc.

ExpressCard — ExpressCard™ is a hardware standard to replace PC Cards (PCMCIA cards), both developed by the Personal Computer Memory Card International Association. Both PCI Express and USB 2.0 connectivity are available to the ExpressCard slot, and each card uses whichever interface the designer feels most appropriate to the task.

The ExpressCard solution accommodates the replacement of conventional parallel buses for I/O devices with scaleable, high-speed serial interfaces. Two classes of serial interfaces are

implemented by this solution, PCI Express, a high performance, integrated I/O interconnect solution, and USB for the ease of upgrading PC Card technologies and integrating popular external peripheral functionality via the ExpressCard module form-factor.

The ExpressCard standard builds on the success of the PC Card Standard, including the 16-bit PC Card and the popular CardBus 32-bit PC Card. ExpressCard technology uses a simpler connector and eliminates the CardBus controller by using direct connections to PCI Express or USB ports in the host. This lowers the cost of slot implementations in host systems.

I²C — The Inter-Integrated Circuit bus (I^2C) is a patented interface developed by Philips Semiconductors. The I^2C bus is a half-duplex, synchronous, multi-master bus requiring only two signal wires: data and clock.

Lane — A PCI Express link is built around dedicated unidirectional couples of serial (1-bit), point-to-point connections known as "lanes". PCI Express lanes are full-duplex links, meaning that data can be transferred in both directions simultaneously (Tx transmit and Rx receive lines are separate).

Link — A connection between any two PCI Express devices is known as a "link", and is built up from a collection of one or more lanes. All devices must minimally support single-lane (x1) link.

LPC Bus — The Low Pin Count Bus is used on embedded PCs to connect low-bandwidth devices to the CPU, such as the boot ROM and the "legacy" I/O devices. The "legacy" I/O devices usually include serial ports, parallel ports, keyboard, mouse, and floppy disk controller. Designers will benefit from the reduced pin count because it uses less space and power, and is more thermally efficient compared to Industry Standard Architecture (ISA) bus.

The LPC specification defines seven mandatory signals required for bidirectional data transfer. Four of these signals carry the multiplexed address and data. The other three are control signals (frame, reset, and clock).

PCI Express — It is a high-speed computer expansion card interface designed to replace the general-purpose Peripheral Component Interconnect (PCI) expansion bus and is software compatible with PCI in order to be transparent to system software. It is structured around point-to-point full duplex serial links called lanes. In PCI Express version

1.1 (currently the most common version), each lane operates at a data rate of 250 MB/s in each direction.

PCIe — Abbreviation for PCI Express.

QMS/QFS — Samtec's micro high-speed connector terminal system.

SBC — Abbreviation for Single Board Computer.

SMBus — System Management Bus is a simple two-wire bus, derived from I²C and used in the x86 architecture for communication with low-bandwidth devices such as memory sticks, clock generators, and temperature sensors.

SPI — The Serial Peripheral Interface Bus is a synchronous serial data link standard named by Motorola that operates in full duplex mode.

SUMIT™ — Abbreviation for Stackable Unified Module Interconnect Technology.

USB — The Universal Serial Bus is a serial bus designed to allow peripherals to be connected using a single standardized interface which replaces certain legacy varieties of serial and parallel ports.

uWire — Microwire is a three-wire synchronous interface developed by National Semiconductor. The Microwire protocol is essentially a subset of the SPI interface. Microwire/Plus with alternate shift clock is compatible with SPI mode 0. Microwire with standard shift clock is compatible with SPI mode 1.

3.0 Connector

3.1 QFS/QMS Micro High Speed Series

As boards and systems get smaller and as the number of small form factors proliferates, it has become more important to focus on robust, high-speed connector technologies. The connector system must be able to handle high-frequency signals required by PCI Express and USB, and must be available off-the-shelf as a standard product. The connector must also have closely spaced pins (fine pitch) in order to minimize the board space consumed by the connector. In addition, the connector of the mated pair that better protects the pins when expansion I/O boards are not used, shall be on the top surface of CPU boards and I/O boards.

These requirements are met by the Samtec QFS/QMS Micro High Speed Series with a 0.635 mm (0.0250-inch) pin pitch. It is a 1-bank terminal assembly that provides a ground blade in the center of the connector. The center ground blade

is important because it provides the return reference for all the high-speed signaling on the SUMIT connector. The QFS standard part number is ASP-129646-01 and the QMS standard part number is ASP-129637-01. The detailed data sheets can be found at http://www.samtec.com/search/sumit.aspx.

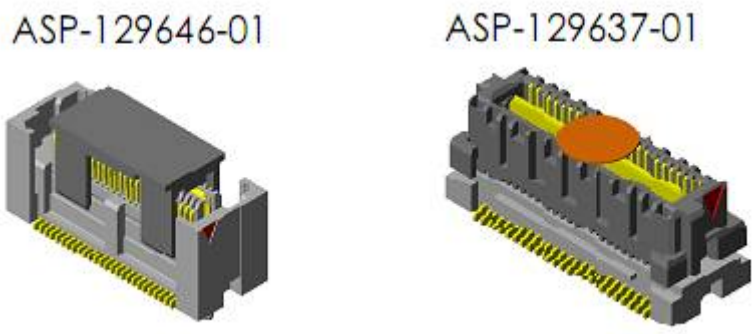


Figure 1: SUMIT mating connector pair

The connector's gold plated pins are mounted in a double row configuration. A total of 52 pins are available per connector. With two connectors, a total of 104 pins are available.

Tests were conducted by Samtec's Signal Integrity Division and the data can be reviewed at www.sff-sig.org. SUMIT can support Generation 2 PCI Express data rates of 5 GT/s. Therefore, the 480Mbps data rate for USB 2.0 plus slower signaling rates for LPC, SPI, and SMBus (I²C) are supported as well.

3.1.1 Connector Stack Height

The stack height is measured from the top of one board to the bottom of the next. Currently stack heights are defined for 15.24 mm (0.600-inch) and 22 mm. For multiple stacking modules, the 15.24 mm is the standard height; however, for a SBC that needs additional clearance for a heat sink, fan or cooling solution, the 22 mm connector can be used. Only the elevated QMS connector mate, ASP142781-01, is needed for 22 mm spacing. The ASP-129646-01 QFS connector remains the same for both 22 mm and 15.24 mm stack heights.

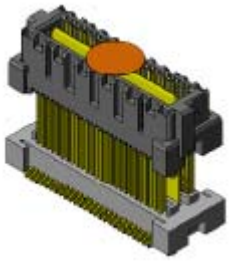


Figure 2: SUMIT 22 mm QMS connector

For the most rugged configurations, those that use stand offs between boards, both the 15.24 mm and 22 mm versions of the QMS/QFS connector pair have been specifically engineered to optimize manufacturing tolerances of this hardware and their buildup in both multiple module stacks and mezzanine implementations.

3.1.2 Connector Placement

The QMS is the top side connector and the QFS is the bottom side connector for SUMIT-based boards. "Top side" refers to the upward facing side of the circuit board for CPU boards as well as for I/O boards, which is usually the major component side of the board. "Bottom side" refers to the opposite I/O board side, and is typically not used on CPU boards unless there is a downward stacking requirement.

This specification does not address the specific location (placement) requirements for any specific form factor boards. Only the relative location (placement) of one connector to the other is specified to ensure proper routing of signals that are passed from one connector to the other as they continue up in a stacked architecture.

If both SUMIT A and SUMIT B connectors are mounted on a board, they must share a common centerline placement in the connector's long axis for all standard implementations. This insures proper alignment and mating for connectors on the stacking modules. Separation of the two connectors is defined to be 26.50 mm measured from the center of each SUMIT connector. Figure 3 shows an example of connector placement for SUMIT-based boards.

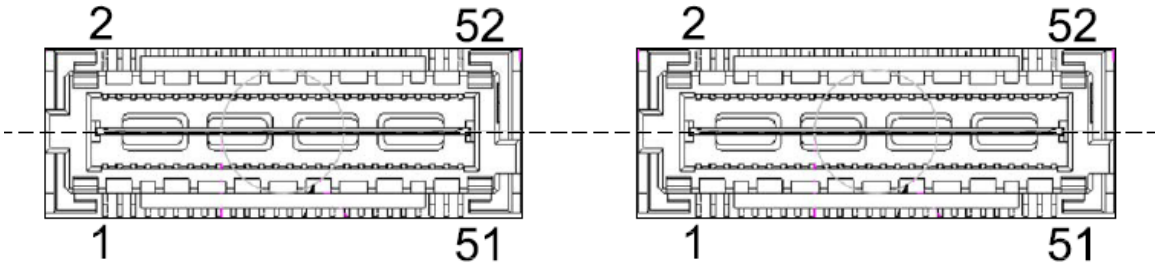


Figure 3: Top side view placement of SUMIT A and SUMIT B connectors

Please refer to the separate form factor specifications for detailed SUMIT connector placement information.

3.1.3 Stacking Order of Expansion Boards

The stacking order for SUMIT-compliant modules is significant due to the high bandwidth of the PCIe lanes. An expansion module with a PCIe x4 lane must be

closest to the root SBC. Next would be an expansion module with a PCIe x1 lane. Stacked above that would be any USB, SPI/uWire, SMBus/I²C, and/or LPC modules. The number of modules in a stack is a function of signal bandwidth, pc board layout and manufacturing processes plus power requirements of each I/O module. The SUMIT connectors have been tested and have the bandwidth to support up to six modules with PCIe Gen 1 devices and a number of other I/O modules using other interfaces added on top if a designer follows the routing recommendations detailed in Section 4.4.

3.1.4 Reserved pins

All reserved pins should pass directly up the stack on the I/O modules. Reserved pins should not be used unless defined by any future SUMIT Specification revisions adopted by the SFF-SIG.

3.2 Connector Configuration Options

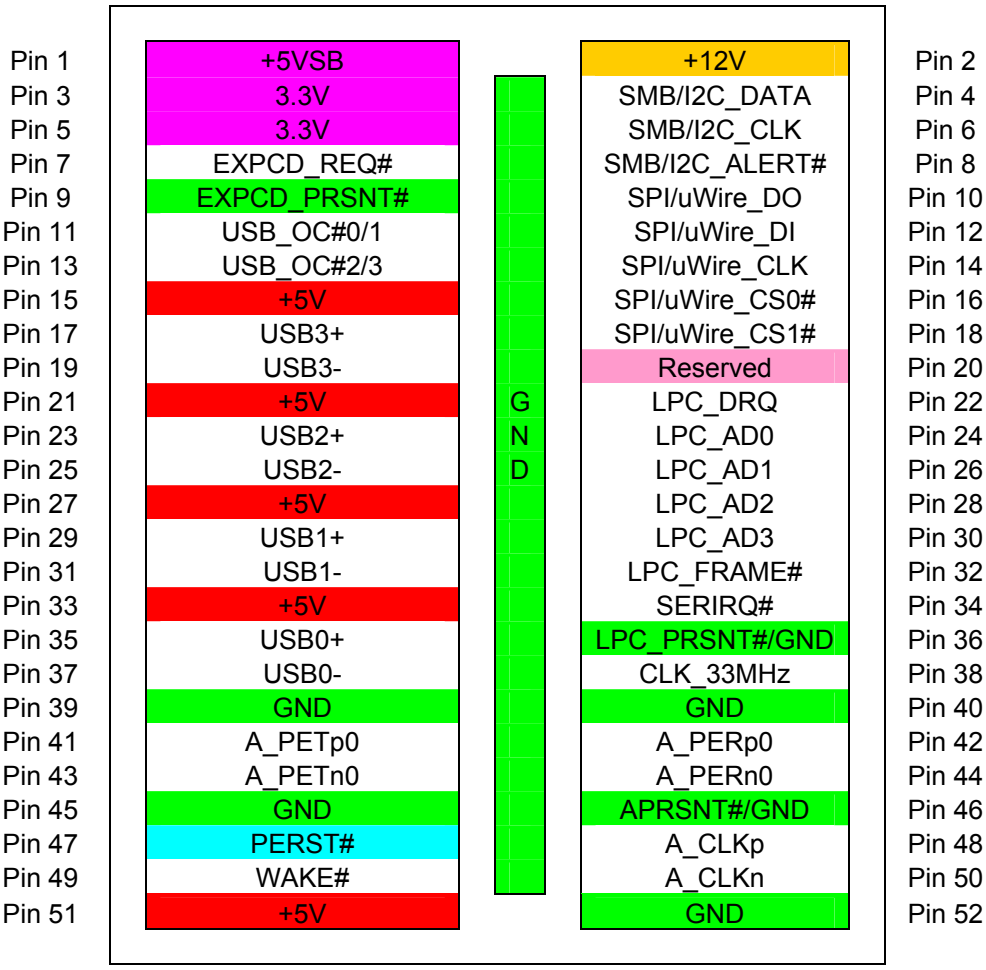
To reduce cost, SUMIT is defined in such a way so that only a single, one-bank connector can be used. This saves printed circuit board space plus the cost of an additional connector if more functionality is not required. By using two smaller, separate connectors instead of one large connector, an expansion or add-in board built with only a single connector can plug directly into other processor or expansion cards populated with both connectors, further reducing overall system cost. For applications only needing one PCIe x1 and one PCIe x4 lane or alternatively a total of five PCIe x1 lanes, only the second connector is needed.

Valid configurations are as follows:

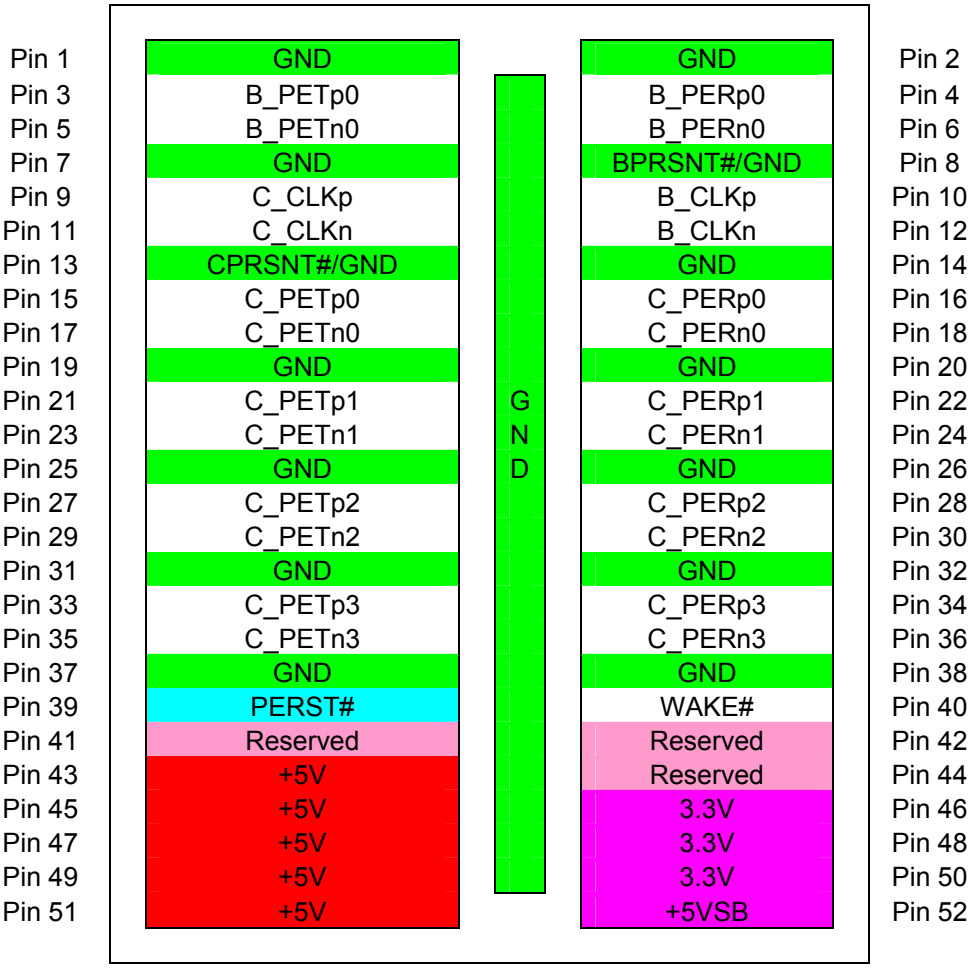
A. Connector A only (pins 1 – 52).
B. Connectors A and B (pins 1 – 52 each, for a total of 104 pins).
C. Connector B only (pins 1 – 52). – This option is "compatible not compliant" meaning that populating only the second connector is completely acceptable. This configuration should not be used in systems where SUMIT-based modules that use the A connector could be installed. The reason is that PCI Express cards must be at the bottom of a stack and not having the first connector in this configuration precludes the "standard" SUMIT configuration.

3.3 Connector Pin Assignments

3.3.1 SUMIT Connector A Pin Assignments



3.3.2 SUMIT Connector B Pin Assignments



3.4 SUMIT Pin Assignments and Descriptions

PCI Express

Signal Name	Connector	Pin #	Description
A_PETp0	A	41	PCIe link A, lane 0, transmit positive pin
A_PETn0	A	43	PCIe link A, lane 0, transmit negative pin
A_PERp0	A	42	PCIe link A, lane 0, receive positive pin
A_PERn0	A	44	PCIe link A, lane 0, receive negative pin
A_CLKp	A	48	PCIe link A, clock positive pin
A_CLKn	A	50	PCIe link A, clock negative pin
APRSNT#/GND	A	46	PCIe link A card present signal (driven by I/O card)
B_PETp0	B	3	PCIe link B, lane 0, transmit positive pin
B_PETn0	B	5	PCIe link B, lane 0, transmit negative pin
B_PERp0	B	4	PCIe link B, lane 0, receive positive pin
B_PERn0	B	6	PCIe link B, lane 0, receive negative pin
B_CLKp	B	10	PCIe link B, clock positive pin
B_CLKn	B	12	PCIe link B, clock negative pin
BPRSNT#/GND	B	8	PCIe link B card present signal (driven by I/O card)
C_PETp0	B	15	PCIe link C, lane 0, transmit positive pin
C_PETn0	B	17	PCIe link C, lane 0, transmit negative pin
C_PERp0	B	16	PCIe link C, lane 0, receive positive pin
C_PERn0	B	18	PCIe link C, lane 0, receive negative pin
C_PETp1	B	21	PCIe link C, lane 1, transmit positive pin
C_PETn1	B	23	PCIe link C, lane 1, transmit negative pin
C_PERp1	B	22	PCIe link C, lane 1, receive positive pin
C_PERn1	B	24	PCIe link C, lane 1, receive negative pin

C_PETp2	B	27	PCIe link C, lane 2, transmit positive pin
C_PETn2	B	29	PCIe link C, lane 2, transmit negative pin
C_PERp2	B	28	PCIe link C, lane 2, receive positive pin
C_PERn2	B	30	PCIe link C, lane 2, receive negative pin
C_PETp3	B	33	PCIe link C, lane 3, transmit positive pin
C_PETn3	B	35	PCIe link C, lane 3, transmit negative pin
C_PERp3	B	34	PCIe link C, lane 3, receive positive pin
C_PERn3	B	36	PCIe link C, lane 3, receive negative pin
C_CLKp	B	9	PCIe link C, clock positive pin
C_CLKn	B	11	PCIe link C, clock negative pin
CPRSNT#/GND	B	13	PCIe link C card present signal (driven by I/O card)
PERST#	A B	47 39	PCI Express reset signal
WAKE#	A B	49 40	PCI Express wake on event signal

USB

Signal Name	Connector	Pin #	Description
USB0+	A	35	USB Channel 0 positive
USB0-	A	37	USB Channel 0 negative
USB1+	A	29	USB Channel 1 positive
USB1-	A	31	USB Channel 1 negative
USB2+	A	23	USB Channel 2 positive
USB2-	A	25	USB Channel 2 negative
USB3+	A	17	USB Channel 3 positive
USB3-	A	19	USB Channel 3 negative
USB_OC#0/1	A	11	USB Channels 0 & 1 overcurrent flag (wire OR)
USB_OC#2/3	A	13	USB Channels 2 & 3 overcurrent flag (wire OR)

ExpressCard

Signal Name	Connector	Pin #	Description
EXPCD_REQ#	A	7	ExpressCard Request
EXPCD_PRSNT#	A	9	ExpressCard Present (driven by I/O card)

SMBus/I²C

Signal Name	Connector	Pin #	Description
SMB/I2C_DATA	A	4	SMBus data
SMB/I2C_CLK	A	6	SMBus clock
SMB/I2C_ALERT#	A	8	SMBus interrupt line in

SPI/uWire

Signal Name	Connector	Pin #	Description
SPI/uWire_DO	A	10	Serial Data Out from Master, 3.3V
SPI/uWire_DI	A	12	Serial Data In to Master, 3.3V
SPI/uWire_CLK	A	14	Serial Clock
SPI/uWire_CS0#	A	16	Chip select for device 0
SPI/uWire_CS1#	A	18	Chip select for device 1

LPC Bus

Signal Name	Connector	Pin #	Description
LPC_DRQ	A	22	LPC DMA request
LPC_AD0	A	24	LPC address, data, and control line 0
LPC_AD1	A	26	LPC address, data, and control line 1
LPC_AD2	A	28	LPC address, data, and control line 2
LPC_AD3	A	30	LPC address, data, and control line 3
LPC_FRAME#	A	32	LPC Frame signal to start or terminate cycles
SERIRQ#	A	34	Serial IRQ for legacy interrupts
LPC_PRSNT#/GND	A	36	LPC card present (driven by I/O card)
CLK_33MHz	A	38	33 MHz clock out

Reserved Pins

Signal Name	Connector	Pin #	Description
Reserved	A B	20 41, 42, 44	These signals are reserved for future use and should *not* be used.

Power and Ground

Signal Name	Connector	Pin #	Description
+5V	A A B B	15, 21, 27, 33, 51 43, 45, 47, 49, 51	+5 volt power
+5VSB	A B	1 52	Standby +5V (for ATX-style)
+3.3V	A B	3, 5 46, 48, 50	+3.3 volt power
+12V	A	2	+12 volt power
Ground	A A B B B B A and B	39, 40 45, 52 1, 2, 7, 14 19, 20, 25, 26, 31, 32, 37, 38 Center blade	Ground. Note that the center conductor blade in both connectors is ground.

Note: Ground is also present when the PRSNT# signal is asserted by I/O cards that support PCI Express, LPC, and ExpressCard. This ground aids in preventing cross talk on adjacent signal pairs. These signals are as follows:

Signal Name	Connector	Pin #
APRSNT#/GND	A	46
BPRSNT#/GND	B	8
CPRSNT#/GND	B	13
EXPCD_PRSNT#	A	9
LPC_PRSNT#/GND	A	36

Note: SUMIT signal levels are active high unless the signal name is appended with the "#" symbol which indicates active low. The USB and PCIe data lines are differential.

Note: Certain chipsets do not support all the interfaces defined by SUMIT. If a vendor's board does not or cannot support one or more of the interfaces, it should be clearly marked in their data sheet and technical manuals.

3.5 SUMIT Connector Physical Specifications

Materials	Spec
Housing:	LCP (Liquid Crystal Polymer) Thermoplastic, UL Rated 94-V0
Contact:	Phosphor bronze
RoHS Compliant:	Yes

Contact Finish	Spec
Socket Interface:	30 micro-inches Gold On Contact Area
Terminal Interface:	30 micro-inches Gold On Contact Area
Underplate:	50 micro-inches Minimum of Nickel

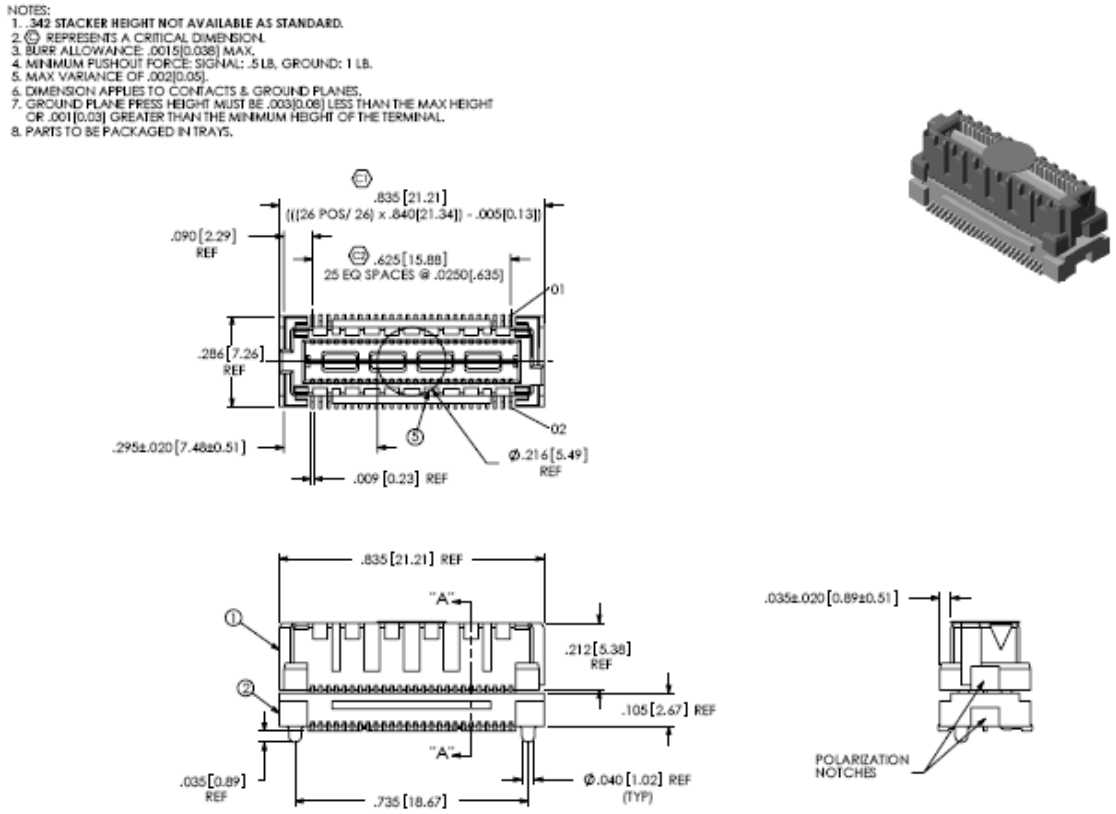
Mechanical Performance	Spec
Insertion Force, One-bank:	3.4 lbs. typical
Withdrawal Force, One-bank:	2.9 lbs. typical
Normal Force:	69 gr. @ 0.006 Inches Deflection
Durability:	1000 Cycles
Operating Temp:	-55°C to +125°C

Electrical Performance	Spec
Contact Resistance:	27.9 milliohms max.
GND Resistance:	5.0 milliohms max.
Contact Current Capacity:	1.5 A @ 30°C Temp Rise
GND Current Capacity:	7.2 A @ 30°C Temp Rise
Dielectric Strength:	1125 VAC
Insulation Resistance:	5,000 Meg Ohms Minimum

Solderability	Spec
Processing Temperature:	260°C produces no blistering, distortion, or discoloration

High Frequency Performance	Spec
Single-Ended System Impedance:	50 Ohms ±10%
Differential Pair System Impedance:	100 Ohms ±10%
Differential Performance:	5 GHz @ -3db insertion loss

3.6 QMS Connector Drawings



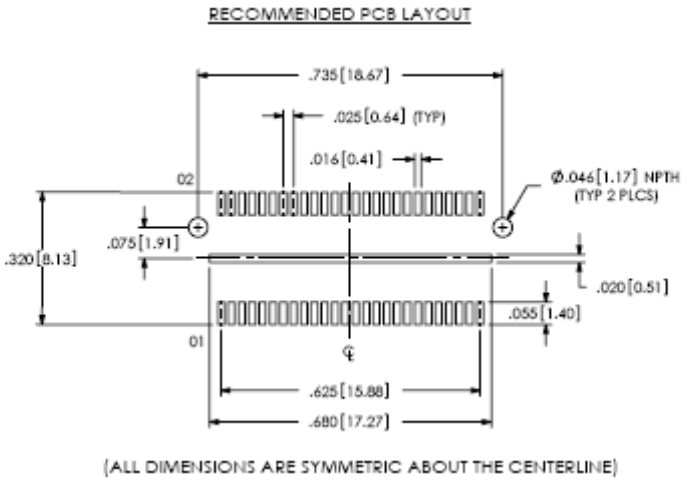
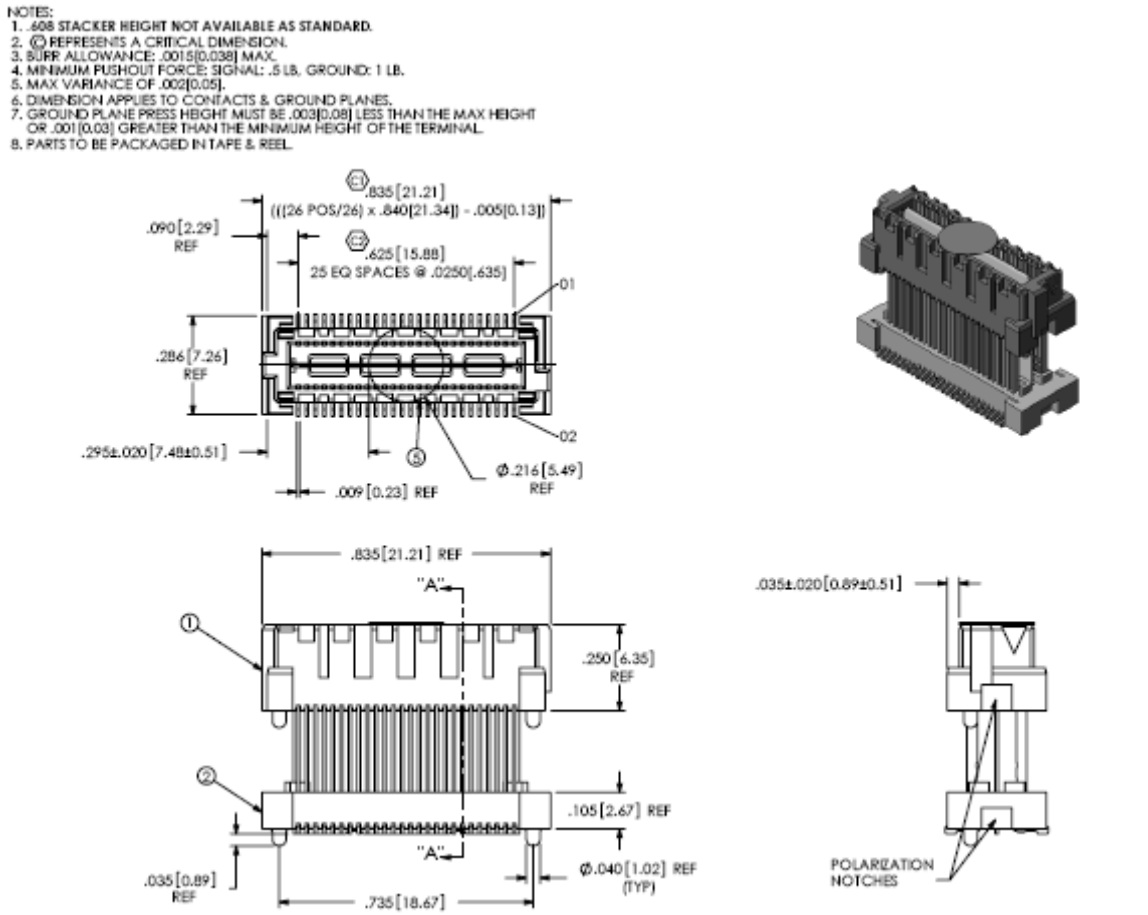


Figure 4: 15.24 mm Stack height QMS Connector



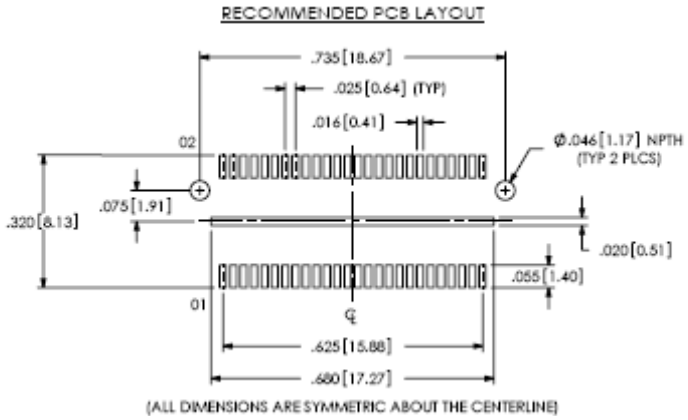
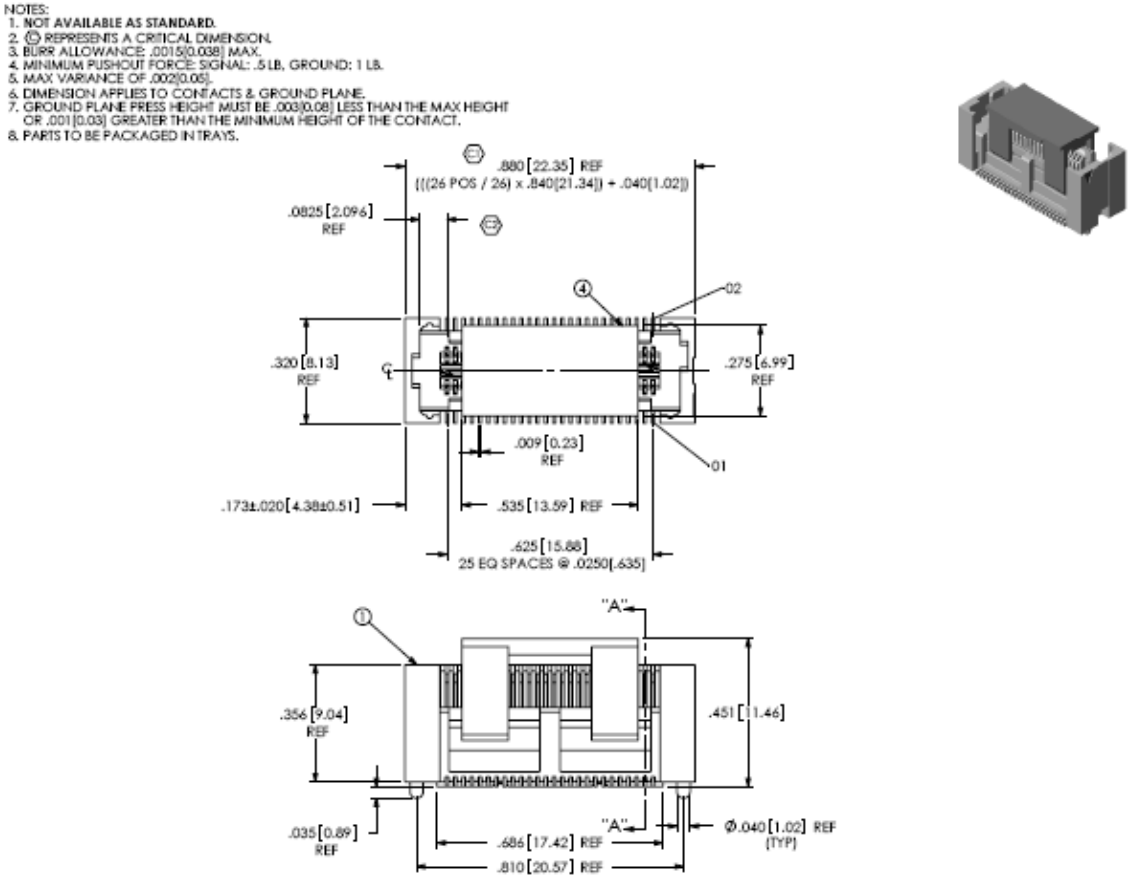


Figure 5: 22 mm Stack height QMS Connector

3.7 QFS Connector Drawings



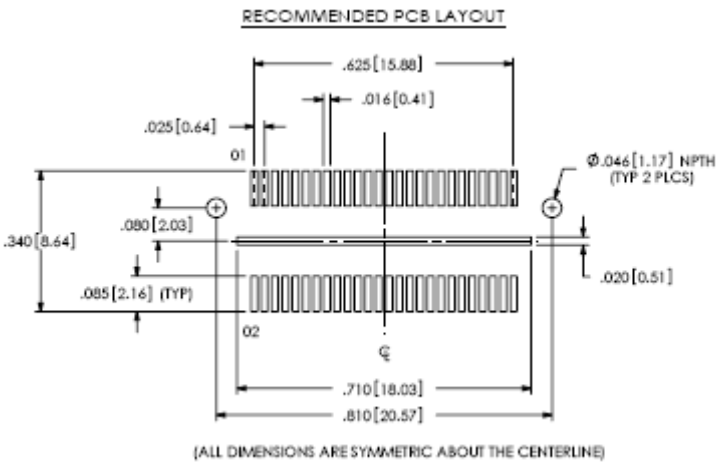


Figure 6: SUMIT QFS Connector

4.0 RECOMMENDED DESIGN PRACTICES

4.1 Implementing SUMIT

Products designed with SUMIT technology can have a number of different interconnect buses in a single connector. Ultra-high speed, high speed, and moderate-to-low speed interfaces can easily coexist on a single connector by using the recommended layout guidelines. A single expansion module can contain devices connected to all of the supported interfaces. However, another single expansion module could contain a device using only one of these interfaces, while passing the unused signals up the bus for additional expansion in a stackable architecture.

Considerable effort has been made to ensure that routing on both processor and expansion modules is efficient, plus consideration to design rules and limitations for each respective interface has been given. One connector's placement with respect to the other is made such that cards passing signals up the bus can do so effectively with ease of layout and signal integrity as primary goals. This "passing" of signals "up the bus" is analogous to the way PCI interrupts have been routed in a rotating method on PC motherboards for more than a decade. Cards can use one or more resources from their connector while the remaining resources are routed to other connectors, justified back to the first pin. All expansion modules are exactly the same from the connector pin-out perspective.

The following section is intended to help the designer identify areas for special consideration and further research. This design guideline should by no means be considered a complete reference, only a reasonable starting point. Following these guidelines does not guarantee a successful design. There are many sources available that discuss high-speed printed circuit board design, USB, or PCI Express specific design guidelines. The following is no way an attempt to repeat this information or instruct the designer in these areas. It merely touches on general guidelines that should be observed, as well as some SUMIT-specific design rules.

Any designer building an SBC or expansion product with SUMIT technology should refer to the "Related Documents and Organizations" in section 1.3 of this specification for links to applicable specifications and their governing bodies.

4.2 SUMIT General Routing Recommendations

SUMIT supports several common interfaces for low to moderate speed expansion requirements. Industry standard serial interfaces include SMBus, I^2C, SPI, and Microwire. SMBus alert is included for power management alert functionality or general SMBus interrupt usage. Two chip selects are included for SPI/uWire, which can be expanded within the target device to any number needed. SPI is defined as 3.3V signaling. 5V tolerant SPI devices may be used

as long as they do not drive the SPI signals on the bus beyond the 3.3V nominal specification. If more bandwidth is required, an LPC bus interface is also available on Connector A that includes SERIRQ signaling for interrupts. The LPC interface directly provides support for LPC and FWH (firmware hub) devices, as well as the only remaining embedded interconnect solution for support of legacy ISA devices on new processor products. A simple bridge chip on the target module, or as a transition board in the stack, is all that is required for ISA.

Routing for all of these interfaces falls into “best design practice” for standard printed circuit board layout. For more specific information, refer to the parent specification or each interface referenced in section 1.3, or to data available from the manufacturer for the targeted device implemented.

4.3 SUMIT USB Routing Recommendations

SUMIT supports four USB signal pairs routed through the A connector. Also, two overcurrent signals for the four ports are included in the same connector.

With a -3db specification at 5 GHz, SUMIT is USB speed independent. As of the release of this specification, all speeds of USB signaling are compatible with the connectors used in SUMIT. Both the manufacturer of the SUMIT connected USB host card and the SUMIT connected USB target must design to the respective specifications of the device used. USB OTG (On-The-Go) compatible devices may also be implemented with SUMIT.

General routing recommendations and considerations for USB are commonly available. SUMIT-specific implementations only need to ensure that these are met, and to observe the recommendations below.

Recommended USB Implementation Guidelines:

- Use USB specific, active power switching devices located directly at the device or connector leading off board. The use of polyfuse type protection circuitry is acceptable but less desirable than active switches in embedded systems because of the fast acting and in-rush limiting qualities of active devices. Omitting protection for off board devices is strongly discouraged.
- For designers of devices that consume more than 500 mA @5V continuous, refer to section 4.6 and to the specific SUMIT-enabled form factor specifications for system power considerations.
- Ample bypassing and bulk decoupling for off board devices is mandatory to prevent system brown out or reset issues during hot swap or power up.

4.4 SUMIT PCI Express Routing Recommendations

SUMIT supports PCI Express signaling. A single PCI Express x1 interface is available using only Connector A. Two x1 and a single x4 are supported when

using both connectors. One Wake signal per connector, one Card Present for each link, and a separate clock pair for each link is included in the pin definition for SUMIT.

PCI Express requires careful consideration when laying out a processor or I/O expansion board. PCI Express Generation 1 is a 1.25 Gigabit per second differential serial interface. With a maximum edge rate specified at 50 picoseconds, or 7 GHz, routing is critical. Even at realized real world edge rates of ~100 picoseconds, the utmost in attention to detail is required for a successful design.

When designing a printed circuit board for any extremely high-speed differential signaling environment, the symmetry of the circuit is of utmost importance. Matching each segment pair length, matching left hand and right hand turns for the pair, placing vias or components symmetrically in the signal path, and routing the trace pair symmetrically to these features are critical to minimize impedance, reflection, and flight time mismatches that degrade signal quality at these frequencies.

Recommended PCI Express Implementation Guidelines:

- Signal names on the connector are from the context of the processor/chipset. This is consistent with the PCI Express specification. (e.g. PETp0 on the connector is the processor board's PCIe transmit positive pin and should be coupled to the I/O card's PCIe corresponding receive pin)
- 100 ohms ± 20% characteristic differential impedance
- 0.005" trace width, 0.007" space between pairs
- 0.020" minimum space from differential pairs to adjacent conductors
- Match signals of differential pair as closely as possible, 0.005" max per board
- One via per card per signal plus one via each end for breakout
- Vias placed symmetrically in the differential pair path
- Capacitive coupling components placed as close as possible to transmitter and placed symmetrically in the differential pair trace path
- Match number of turns left and right, no sharp or 90 degree turns
- Microstrip routing only over solid planes. (No routing over breaks in planes)
- Stripline routing is not recommended unless using blind or back drilled vias to eliminate the stub
- Match lane to lane length within a link to ± 2.00" on SBC and ± 0.50" on an expansion card
- Maximum lane length on a SBC is 12.00" component to connector
- Maximum lane length on an expansion card is 2.50" connector to component
- Maximum lane length on an expansion card is 1.00" to route up from bottom connector to the top connector as a totem pole pass-through
- Card present signals are grounded on the expansion card for the link(s) consumed only

- Implementations with multiple expansion cards stacked together:
    - PCI Express interface modules must be placed at the bottom of the stack (nearest the processor or host module)
    - The PCIe x4 link should be the first board next to the SBC
    - PCIe x1 links should consume link A first
    - Transmit, receive, clocks, and card present signals for x1 link B are shifted to the link A pins on the top connector, The same from C to B, etc
- Multi-card stacked implementations including connector B that consume the x4 link should leave these signals as no connects on the top connector
- The x4 link can be used as up to 4 x1 links
- Multi-card stacked implementations including Connector B that do not consume the x4 link but do use a x1 link should pass the lane 0 signals of link C (i.e. C0) directly up from bottom to top on link B, C1 lanes are shifted from the bottom to C0 lanes on top, etc. Refer to section 4.7 for more information

4.5 SUMIT Express Card Routing Recommendations

The SUMIT specification provides signaling for ExpressCard present and for ExpressCard request. These are the only two additional signals necessary to implement an ExpressCard beyond a x1 PCI Express Link and/or a single USB signal pair.

- ExpressCard interfaced products should follow the USB and PCIe recommended guidelines in this document and from their referenced parent specification.
- In a stacked implementation with multiple expansion cards, boards that consume the ExpressCard interface should conform to the routing recommendations from the USB and PCIe in Sections 4.3 and 4.4.
- Once consumed from the bottom connector, EXPCD_PRSNT# and EXPCD_REQ# on the top connector are not connected.

4.6 Power

The SUMIT specification provides for expansion module power to be supplied through both connectors on designated pins. Ground return is supplied via the center ground contact, and through individual pins in each bank populated. It is highly recommended that switching type power supplies be used to generate any expansion card voltages necessary because of their excellent transient response and their inherently high efficiency.

The SUMIT specification does not specify the minimum power requirement a baseboard must provide to SUMIT I/O modules. This will be specified within each standard form-factor mechanical specification to support the minimum requirements of the specific size and format of SUMIT module. Please see the

individual mechanical form-factor specification for more information. The vendor for the processor board chosen may also dictate a specification that limits the total power available to modules in the stack to somewhat less than the SUMIT or specific form factor specification. Power requirements in excess of the SBC's available power specification, or greater than those listed below for the system level definition, must be supplied by a secondary connector on the expansion card itself.

The following table describes the maximum power available from the system perspective for expansion cards. It is assumed that the processor board is powered from a connector separate from either SUMIT connector.

SUMIT System Power Specifications

Connector A only:	
+5V	6.25 Amps continuous
+5VSB	1.25 Amps continuous
+3V	2.5 Amps continuous
+12V	1.25 Amps continuous

Connectors A and B:	
+5V	12.5 Amps continuous
+5VSB	2.5 Amps continuous
+3V	6.25 Amps continuous
+12V	1.25 Amps continuous

Connector B only:	
+5V	6.25 Amps continuous
+5VSB	1.25 Amps continuous
+3V	3.75 Amps continuous

4.7 PCIe Link Alignment on SUMIT-based Modules

A design feature of SUMIT-based stacking I/O expansion modules is that they do not require jumpers or switches for slot selection. These are normally required with previous generation parallel bus technologies using through hole stacking connectors. By contrast, SUMIT uses a pair of surface mount connectors that allow one or more PCI Express x1 interface peripherals to be mounted on an I/O expansion module stack implementing a point-to-point architecture in a self-stacking design. This feature allows automatic link alignment which eliminates the need for jumpers. Boards not supporting PCI Express simply pass all signals straight up the stack from one connector to another.

Each PCI Express x1 link utilizes the auto-alignment topology. Links that are used by the expansion module are automatically selected and the remaining unused signals are simply shifted down to the consumed link's pins on the top connector for use by the next board. This passing of signals "up the bus" is analogous to the way PCI interrupts have been routed in a rotating method on PC motherboards for more than a decade. Individual cards can use one or more links available from their bottom connector while the remaining links are routed up to the next board, justified back to the first links pins. All expansion modules are wired exactly the same from the connector pin definition perspective.

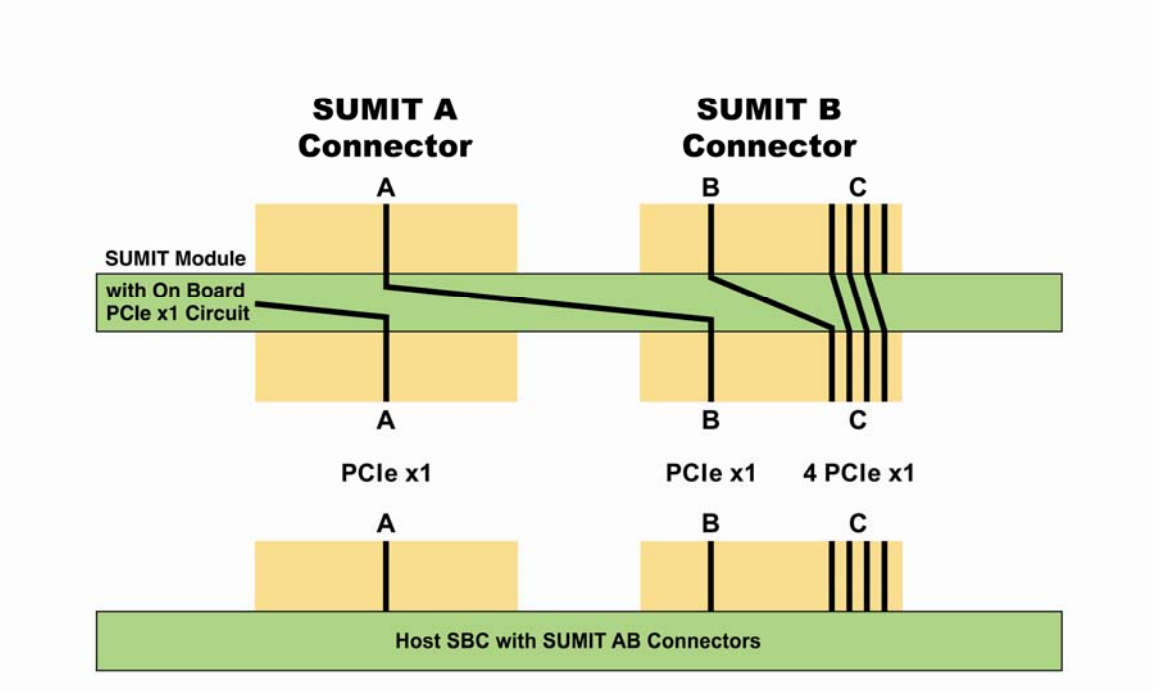


Figure 7: PCI Express auto alignment on SUMIT-based modules

Any SUMIT I/O expansion module with a single x1 PCI Express peripheral is always wired to link A on the "bottom" side connector. On the "top" connector of the same board, the link A pins will be wired from the link B pins on the bottom connector. Link B on the top connector will be wired from link C0 on the bottom, link C0 on top from link C1 on bottom, etc. This is the essence of automatic lane shifting. Link C3 on the top connector will not be used. When passing up any PCIe link, associated clock and presence detect pins for that link must also be auto aligned with the parent signals.

A SUMIT expansion module that utilizes the x4 PCI Express lane has no connections on the top connector for these pins. However, if a module utilizing the x4 link does not use the x1 PCIe links, it passes these signals straight up the bus from top to bottom. When passing through any PCIe x1 link, associated clock and presence detect pins for that link must also be passed up directly with the parent signals.

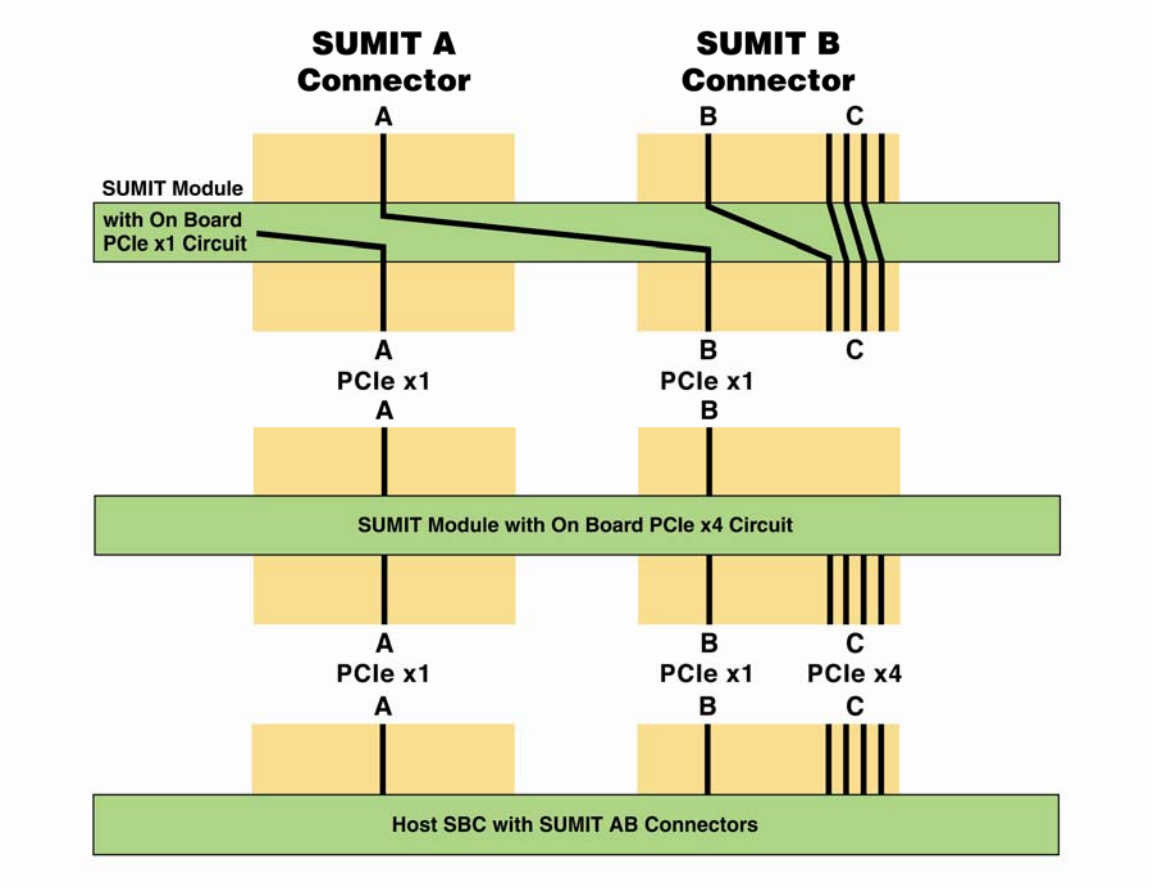


Figure 8: PCIe x1 lane routing on a SUMIT-based module

4.8 Support of Four Additional PCIe x1 Lanes

A host single board computer is permitted to support the current SUMIT PCIe x4 configuration or *optionally* be split into four PCIe x 1 links from the C link pins on the SUMIT B connector. In a SUMIT AB configuration, this would provide up to a total of six PCIe x1 links. Since this alternative is a function of the chipset implementation used in the host SBC design, it is the responsibility of the SBC vendor to clearly specify which configuration was supported in their data sheet and technical documentation. From an I/O module perspective, a designer must auto-align all PCIe x1 links if they use one of the x1 links. USB can similarly be auto aligned for use in the stacking SUMIT architecture. All other signals are

wired to simply pass through straight up the stack from the bottom connector to the top.

To ensure functionality of all interfaces available to expansion modules on SUMIT, a stacking protocol has been established for I/O boards (listed from the first card at the bottom of the stack next to the SBC progressing upward):

(1) If present, one I/O module that consumes a PCIe x4 link
(2) Any number of modules with PCIe x1 Links up to the max available from the SBC
(3) Any number of modules without PCIe support (i.e. LPC, SPI, USB, etc).